1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

DRAWING REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
B		305003	PRODUCTION RELEASED	12/01/03	?

SCHEM,MLB,PB15

Thu Nov 20 18:22:29 2003

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4	PCB NOTES AND HOLES
5	MPC7447 MAXBUS INTERFACE
6	MPC7447 DATA / NC PINS / BOOTBANGER
7	CPU PLL AND CONFIGURATION STRAPS
8	INTREPID MAXBUS AND BOOT STRAPS
9	INTREPID MEMORY INTERFACE / BOOT ROM
10	DDR MEMORY MUXES
11	400PIN STACKED DDR SODIMM CONNECTOR
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIOS/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS/1.5V LDO
16	INTREPID DECOUPLING
17	USB 2.0 INTERFACE (uPD720101)
18	CARDBUS INTERFACE (PCI1510)
19	M10 AGP INTERFACE & SPREAD SPECTRUM SUPPORT External TMDS (DVI Transmitter SIL1162)
20	M10 LVDS/TMDS/GPIO & GPU VCORE
21	M10 POWER

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24	INTERNAL CONNECTORS - AIRPORT, HARD DRIVE, OPTICAL DRIVE
25	FAN CONTROLLER, USB MODEM/SOFT MODEM, SOUND/LEFT USB/BLUETOOTH, SERIAL DEBUG
26	GIGABIT ETHERNET INTERFACE
27	FIREWIRE PHY
28	FIREWIRE PORTS
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41	SIGNAL LOCATIONS
42	COMPONENT LOCATIONS (1 OF 2)
43	COMPONENT LOCATIONS (2 OF 2)

BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
SSCG	NO_SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
USB_MODEM	SOFT_MODEM
GPU_PWRMSR	INT_TMDS
GPU_SS	
VGA_BUFFER_RES	
EXT_TMDS	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6537	1	SCHEM,MLB,PB15	SCH1	
820-1577	1	PCBF,MLB,PB15	PCB1	
065-4722	1	CMNPRT,MLB,PB15	DMS1	DMS630-4874&DMS630-4875
065-4723	1	SELPRT,MLB,PB15,BTR	DMS2	DMS630-4874
065-4725	1	SELPRT,MLB,PB15,BST	DMS3	DMS630-4875

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE NONE	

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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TITLE SCHEM,MLB,PB15"

DRAWING NUMBER 051-6537 REV. B

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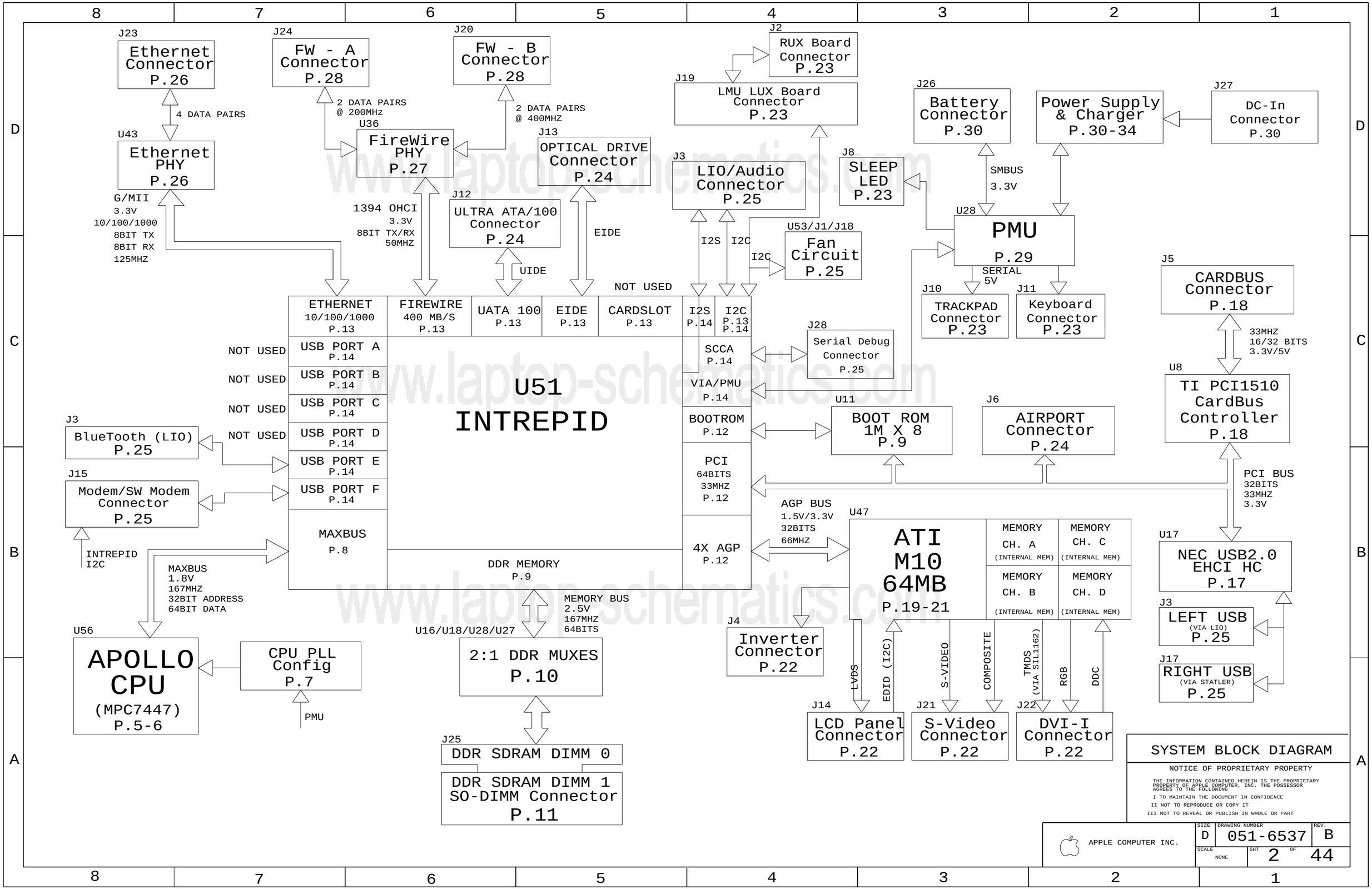

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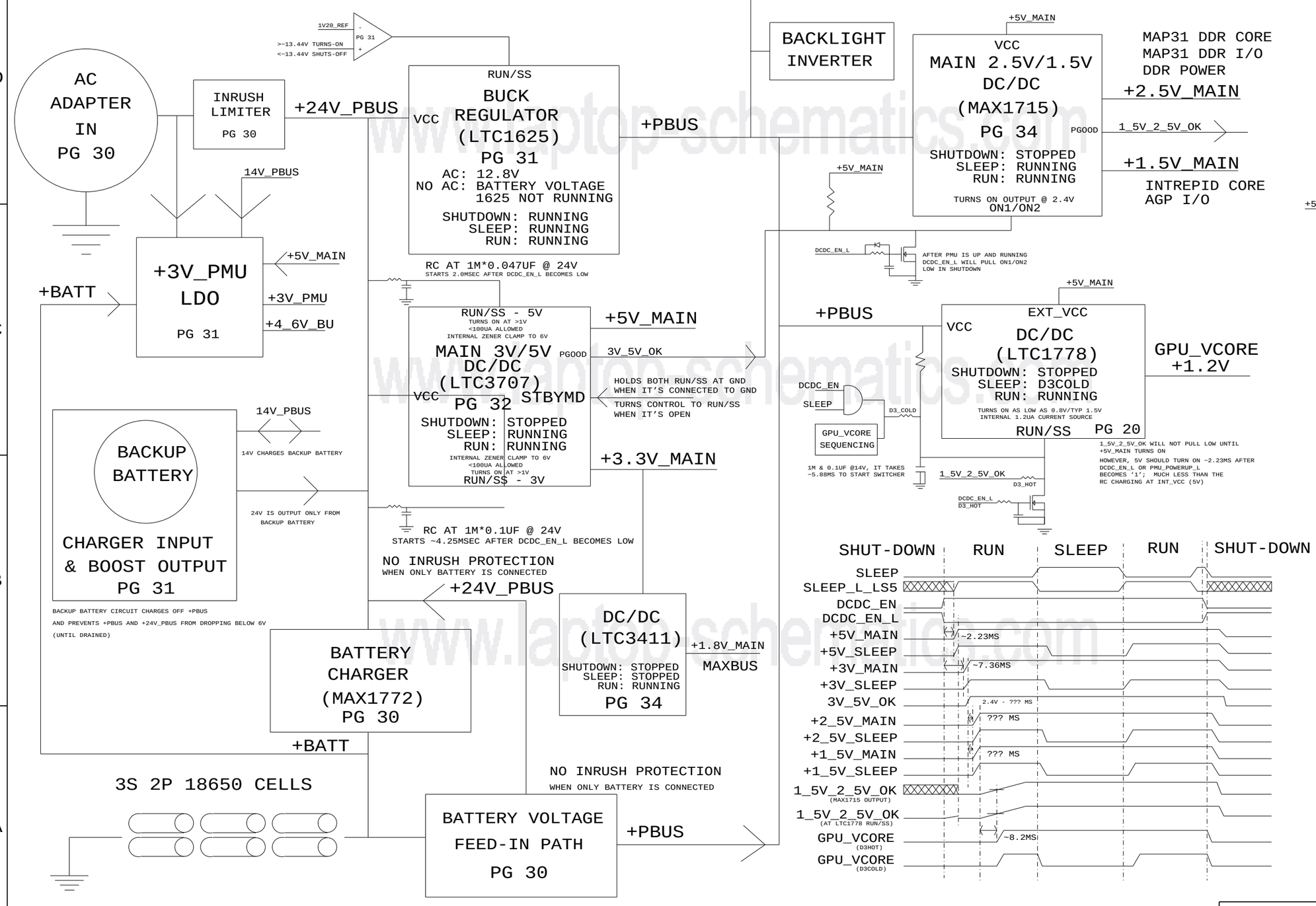
POWER SYSTEM ARCHITECTURE



POWER BLOCK DIAGRAM

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PCB SPECS

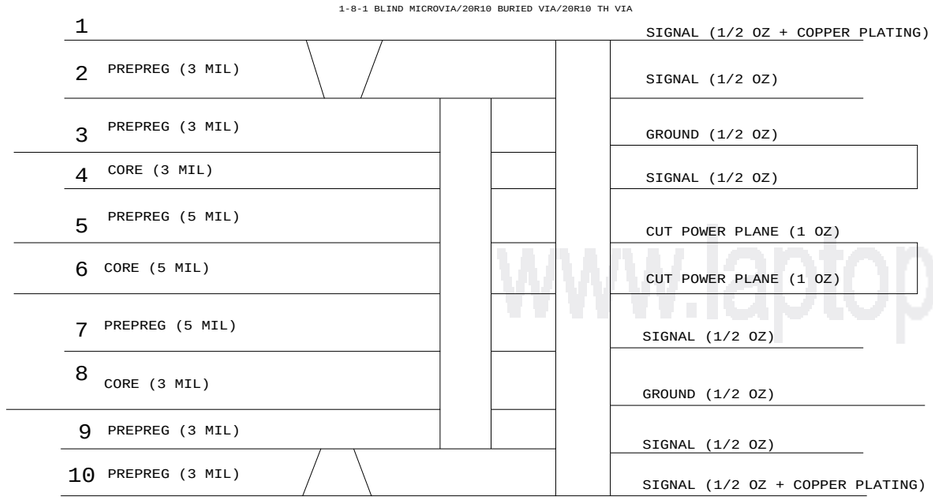
THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

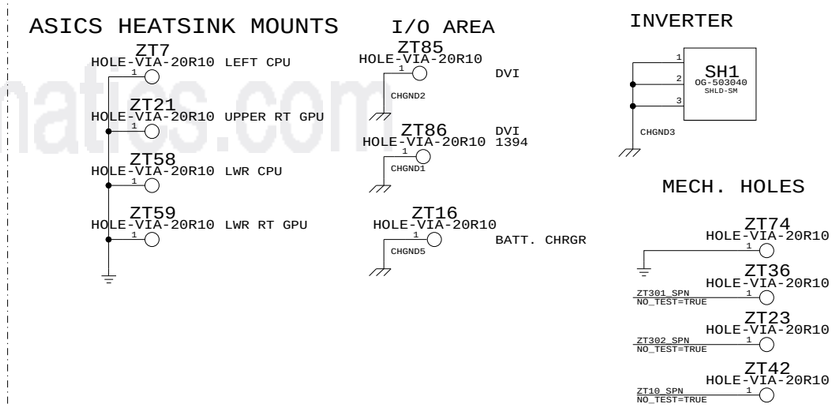
BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA

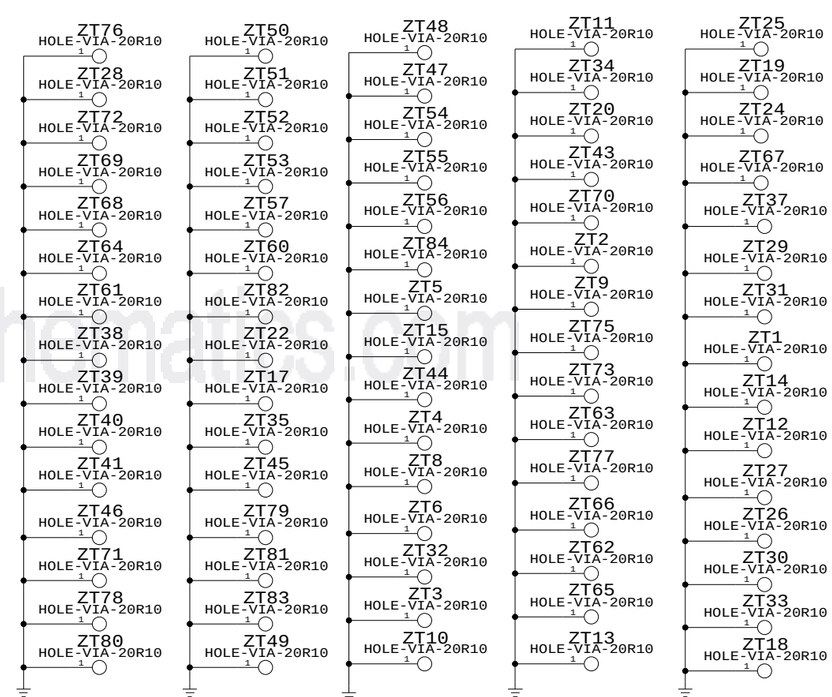


BOARD HOLES

CHASSIS MOUNTS



GROUND VIAS



BOARD INFORMATION

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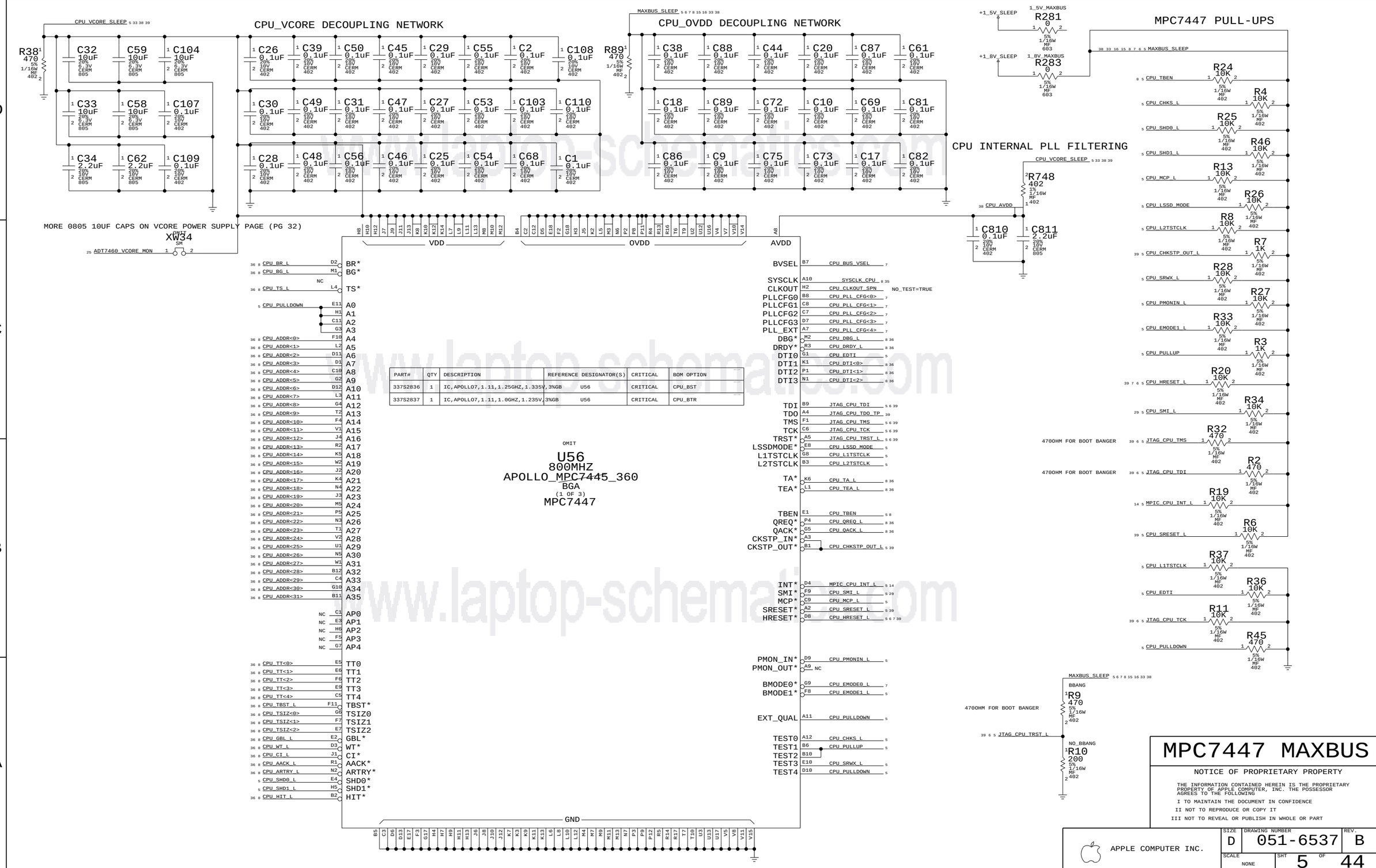

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2836	1	IC,APOLLO7,1.11,1.25GHZ,1.335V,3%GB	U56	CRITICAL	CPU_BST
337S2837	1	IC,APOLLO7,1.11,1.0GHZ,1.235V,3%GB	U56	CRITICAL	CPU_BTR

MPC7447 MAXBUS

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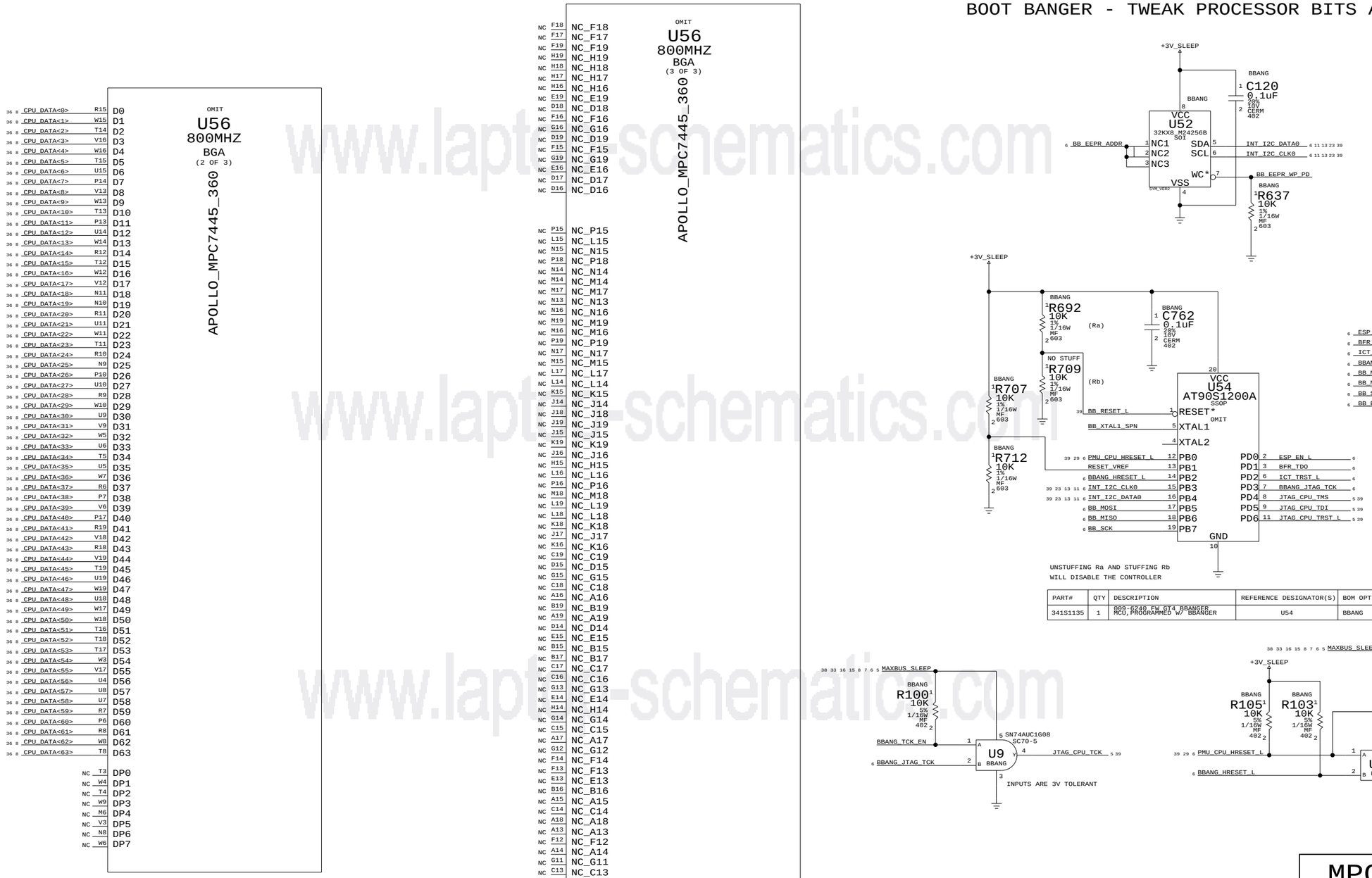
BOOT BANGER - TWEAK PROCESSOR BITS AFTER POWER-ON



UNSTUFFING Ra AND STUFFING Rb
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1135	1	800-8248 FW DT4 BBANGER MCU,PROGRAMMED W/ BBANGER	U54	BBANG

MPC7447/BBANG

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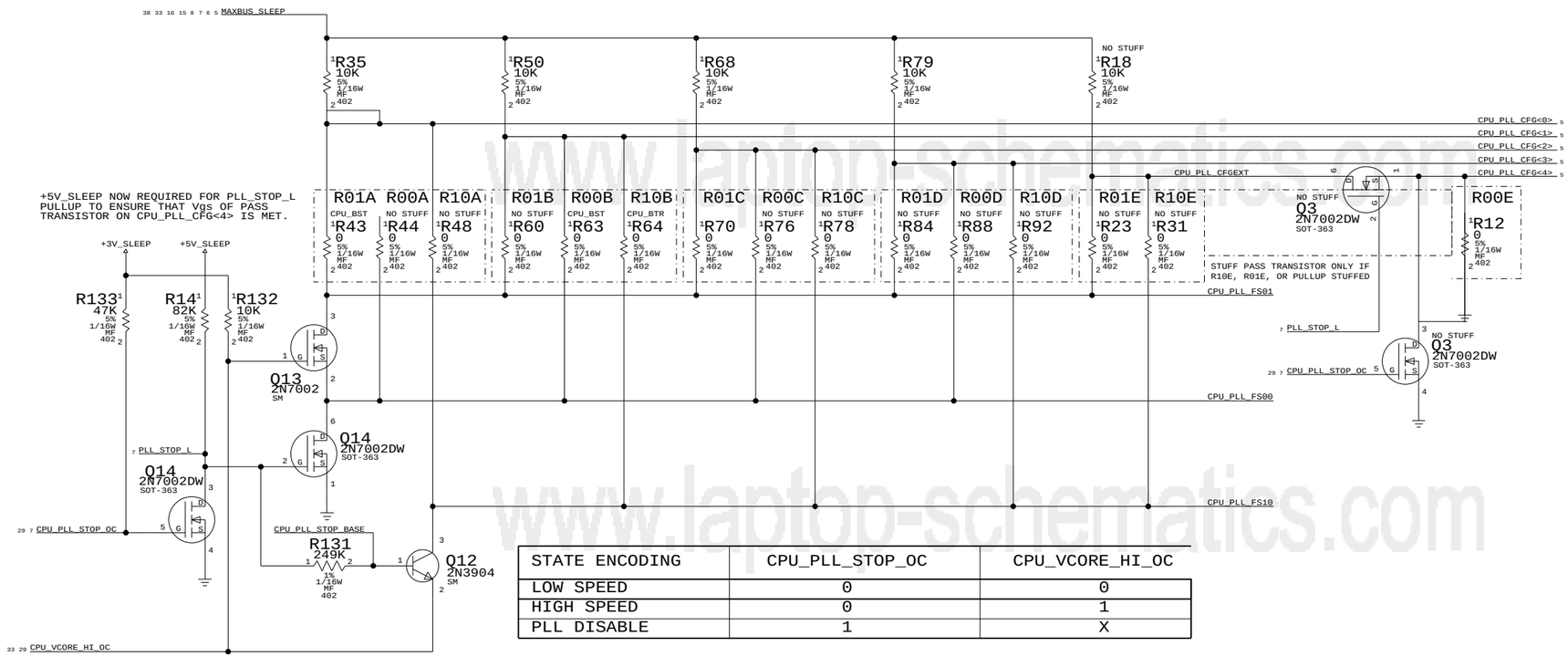
CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

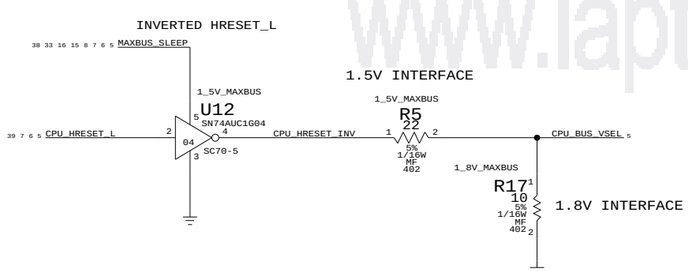
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4	0123	HEX
			E	ABCD	
0.0X	PLL OFF		0	1111	0F
1.0X	PLL BYPASS		0	0011	03
2.0X	333	267	0	0100	04
3.0X	500	400	0	1000	08
4.0X	667	533	0	1010	0A
5.0X	833	667	0	1011	0B
5.5X	917	733	0	1001	09
6.0X	1000	800	0	1101	0D
6.5X	1083	867	0	0101	05
7.0X	1167	933	0	0010	02
7.5X	1250	1000	0	0001	01
8.0X	1333	1067	0	1100	0C
8.5X	1417	1133	0	0110	06
9.0X	1500	1200	1	0111	17
9.5X	1583	1267	0	0111	07
10.0X	1667	1333	1	1010	1A
10.5X	1750	1400	1	1000	18
11.0X	1833	1467	1	1001	19
11.5X	1917	1533	0	0000	00
12.0X	2000	1600	1	1011	1B
12.5X	2083	1667	1	1111	1F
13.0X	2167	1733	1	0101	15
13.5X	2250	1800	0	1110	0E
14.0X	2333	1867	1	1100	1C
15.0X	2500	2000	1	0001	11
16.0X	2667	2133	1	1101	1D
17.0X	2833	2267	1	0000	10
18.0X	3000	2400	1	0010	12
20.0X	3333	2667	1	0011	13
21.0X	3500	2800	1	0100	14
24.0X	4000	3200	1	0110	16
28.0X	4667	3733	1	1110	1E

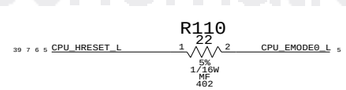
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

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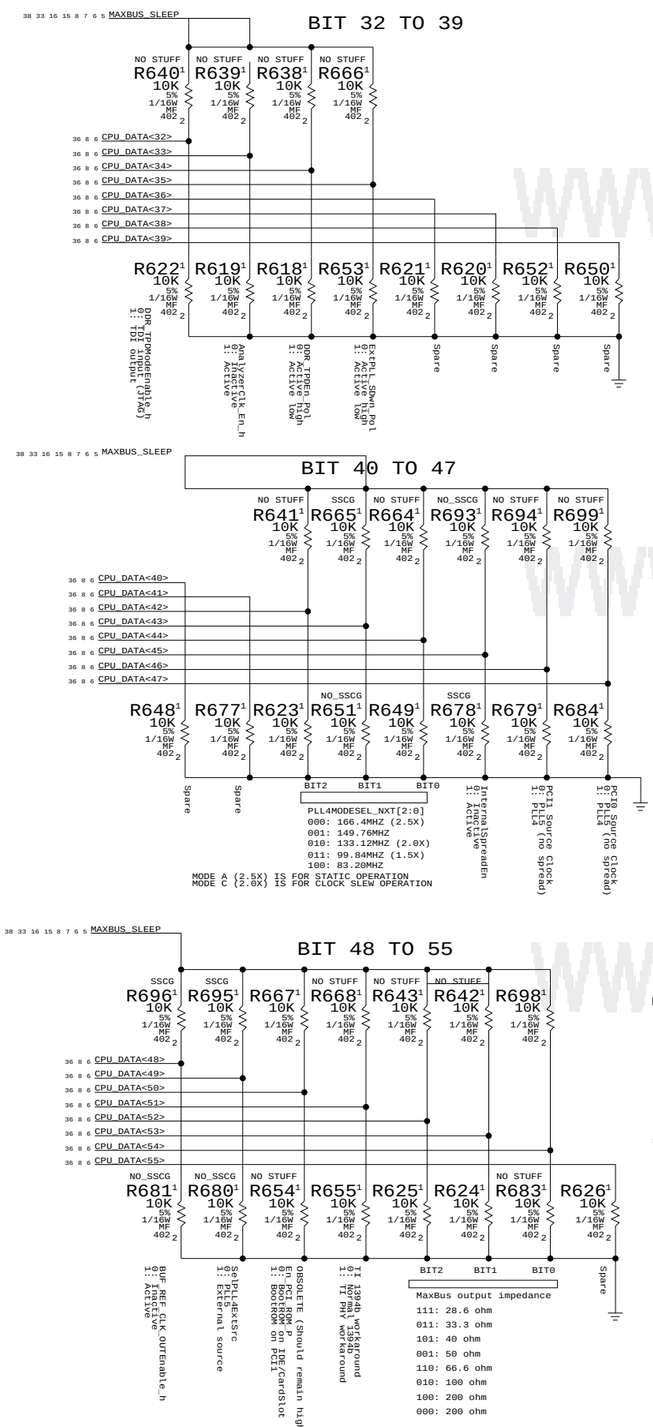
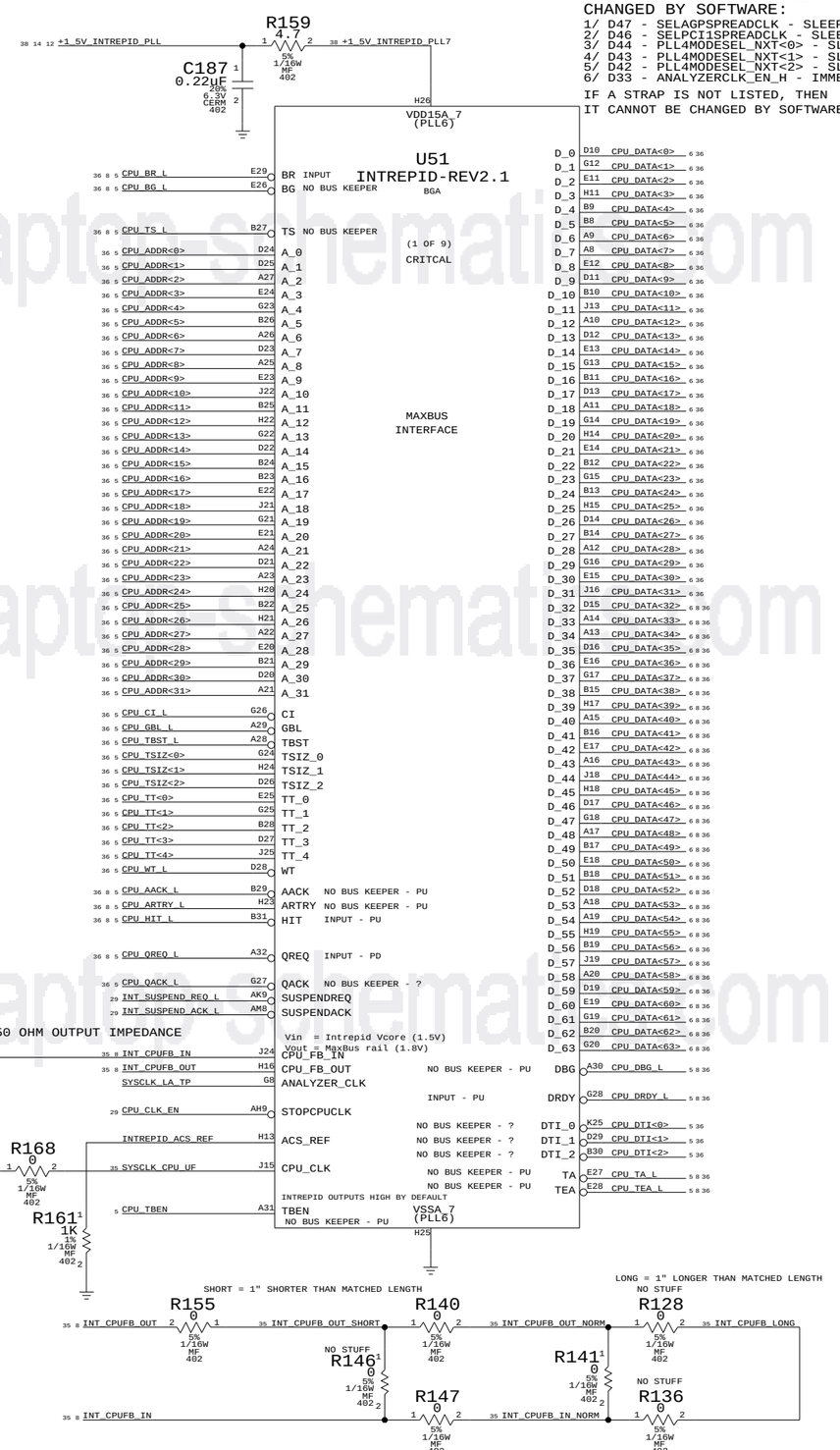
INTREPID BOOT STRAPS



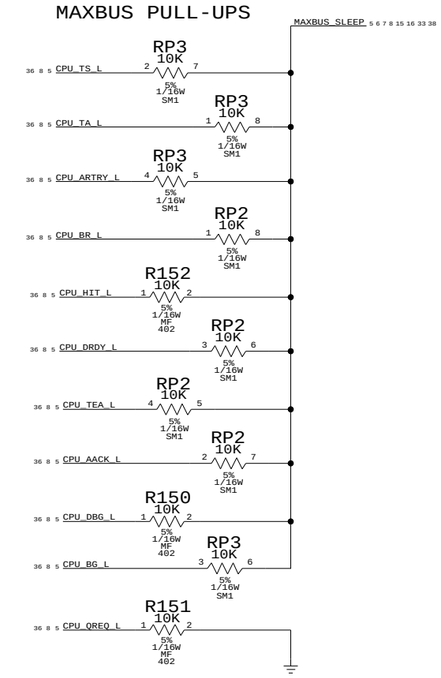
THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

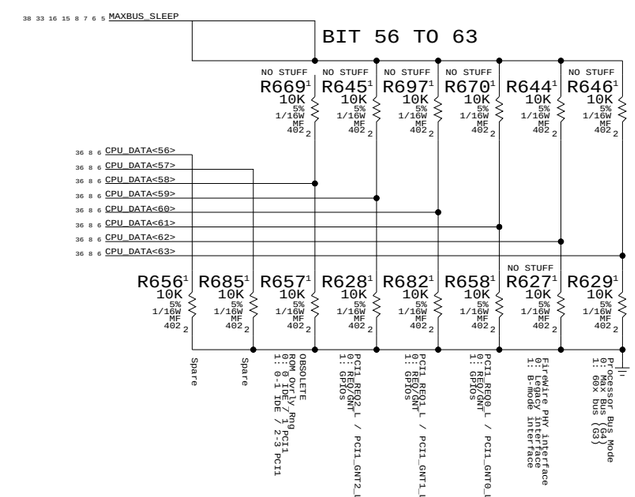
IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE



MAXBUS PULL-UPS



INTREPID BOOT STRAPS



Intrepid MaxBus

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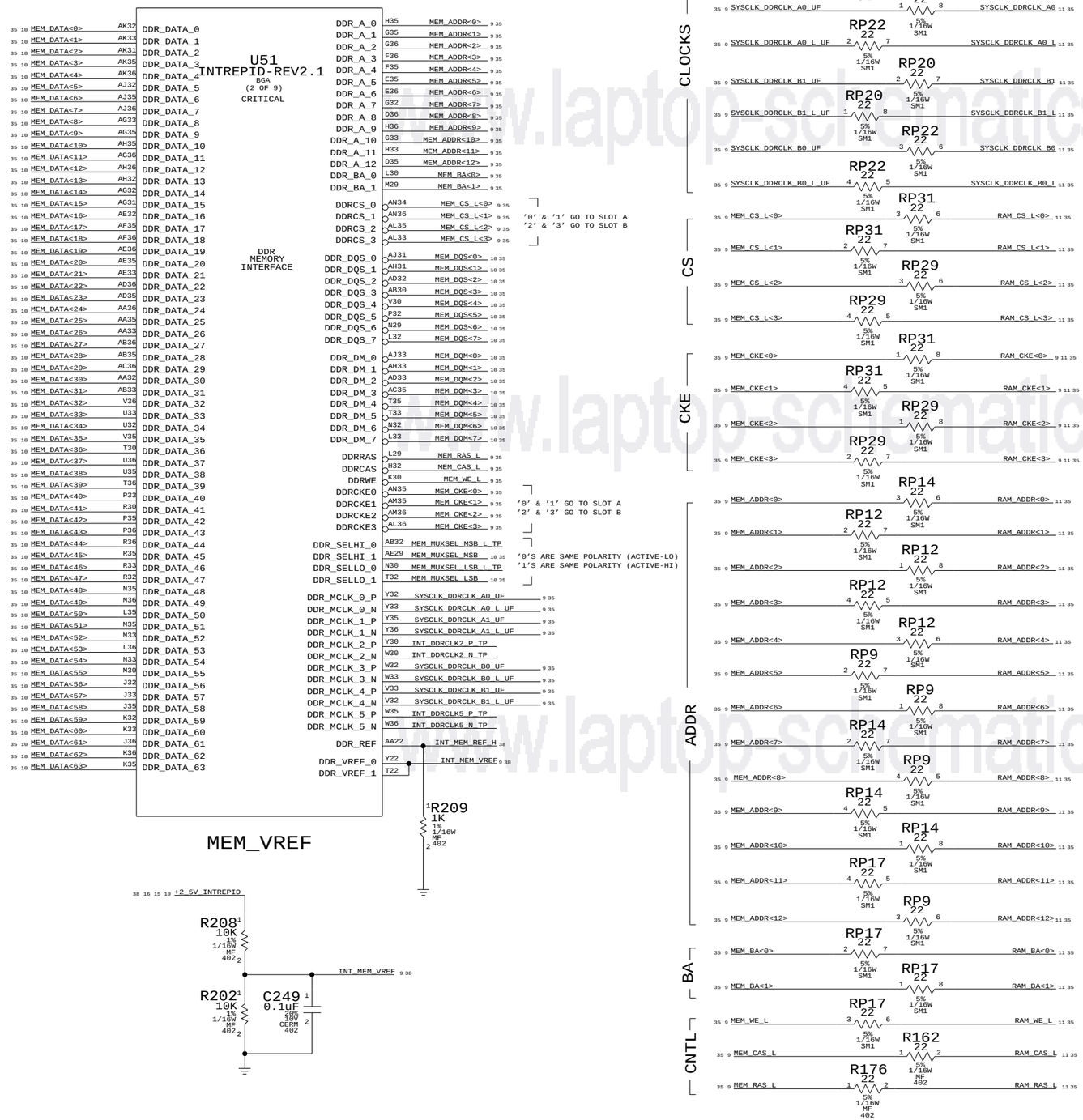
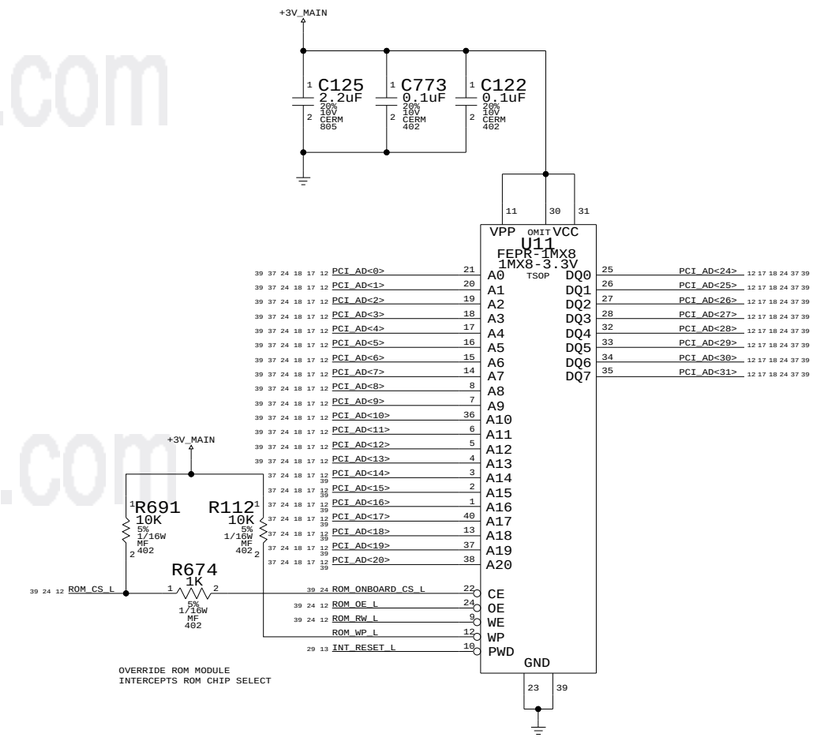
SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

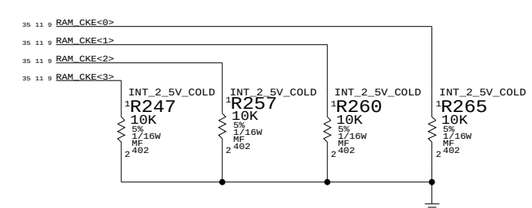


1MB BOOT ROM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1244	1	IC,BOOTROM,Q16	U11		

Weak pulldowns ensure CKEs stay low
after 2.5V I/O to Intrepid shuts off.



INT - DDR/BOOTROM

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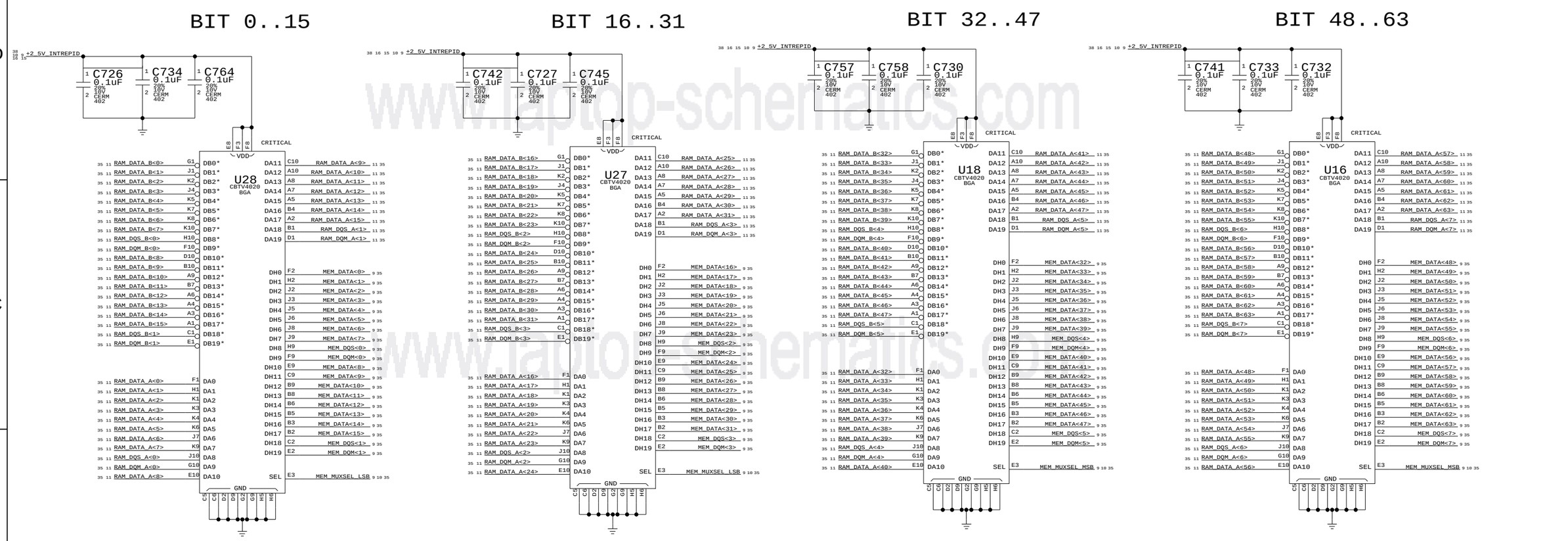

SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

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16BIT 2:1 DDR MUXES

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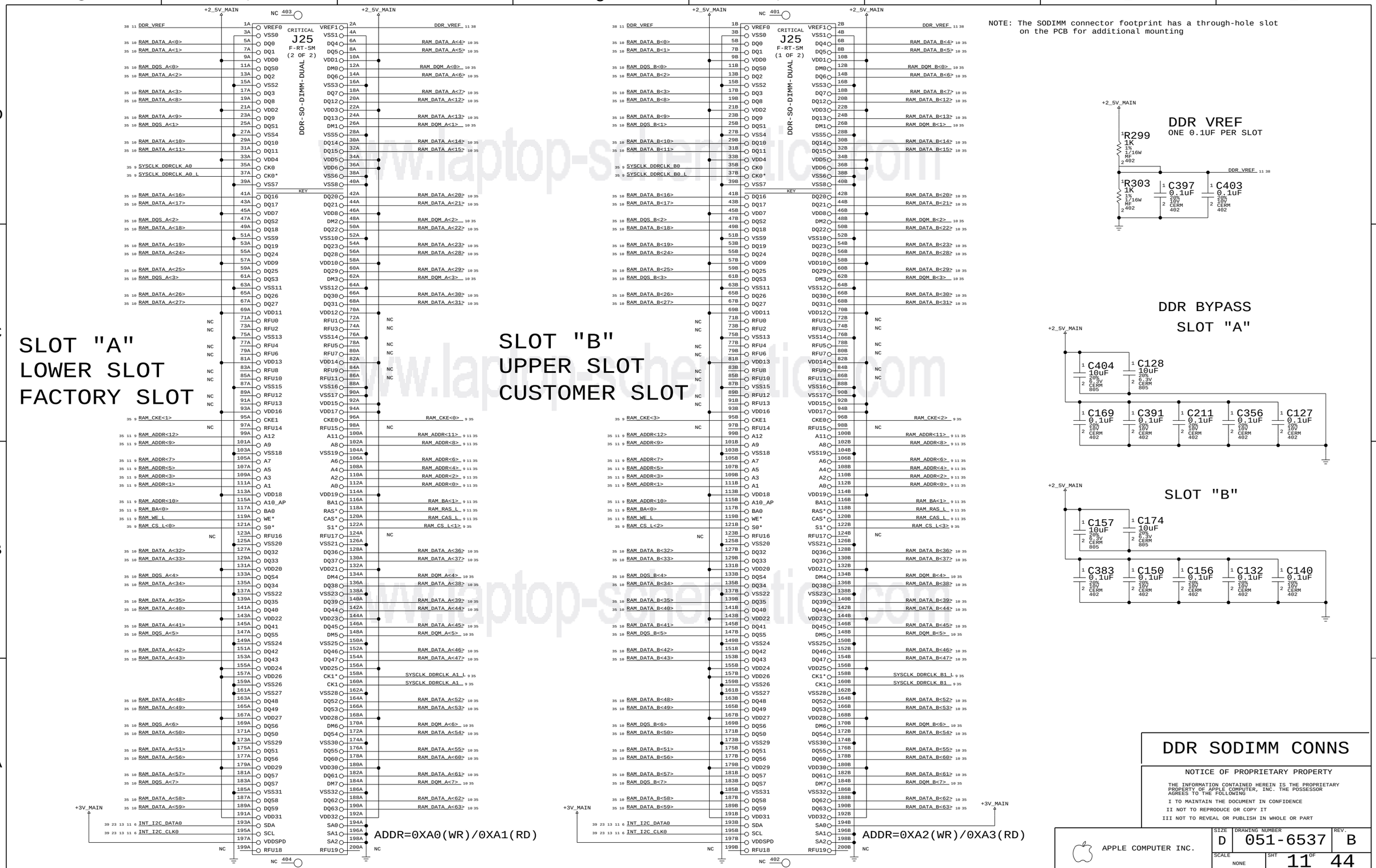

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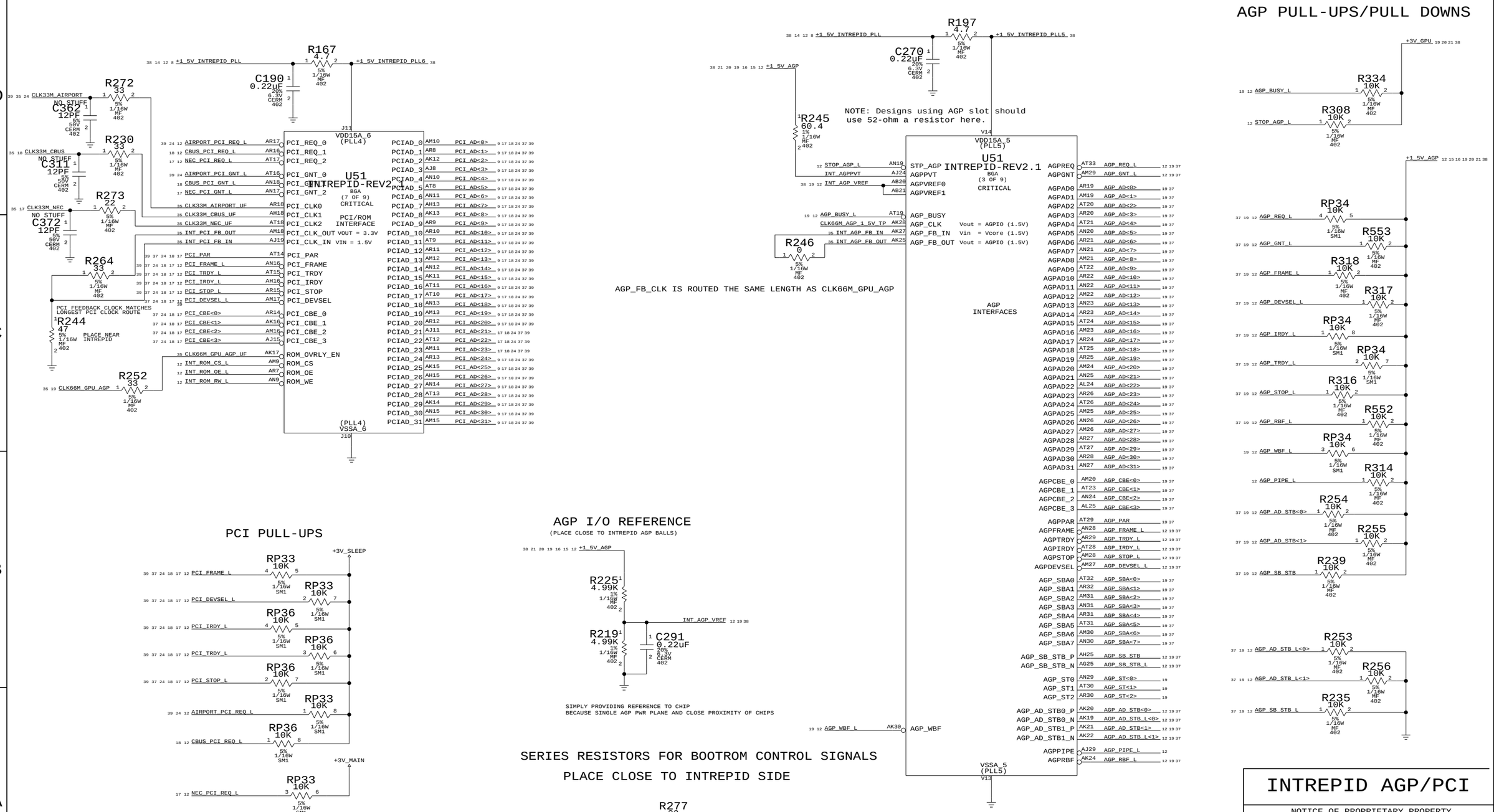
AGP PULL-UPS/PULL DOWNS
PCI PULL-UPS
AGP I/O REFERENCE
(PLACE CLOSE TO INTREPID AGP BALLS)
SIMPLY PROVIDING REFERENCE TO CHIP
BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS
SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS
PLACE CLOSE TO INTREPID SIDE
NOTE: Designs using AGP slot should use 52-ohm a resistor here.
AGP_FB_CLK IS ROUTED THE SAME LENGTH AS CLK66M_GPU_AGP
PCI FEEDBACK CLOCK MATCHES LONGEST PCI CLOCK ROUTE
PLACE NEAR INTREPID
NEC USB2 REQ REMAINS ON +3V_MAIN
BECAUSE THIS CHIP IS POWERED DURING SLEEP
U51
INTREPID-REV2.1
BGA
(7 OF 9)
CRITICAL
PCI/ROM INTERFACE
VDD15A_6 (PLL4)
(PLL4) VSSA_6
U51
INTREPID-REV2.1
BGA
(3 OF 9)
CRITICAL
VDD15A_5 (PLL5)
VSSA_5 (PLL5)
AGP INTERFACES
Vout = AGPIO (1.5V)
Vin = Vcore (1.5V)
Vout = AGPIO (1.5V)
INTREPID AGP/PCI
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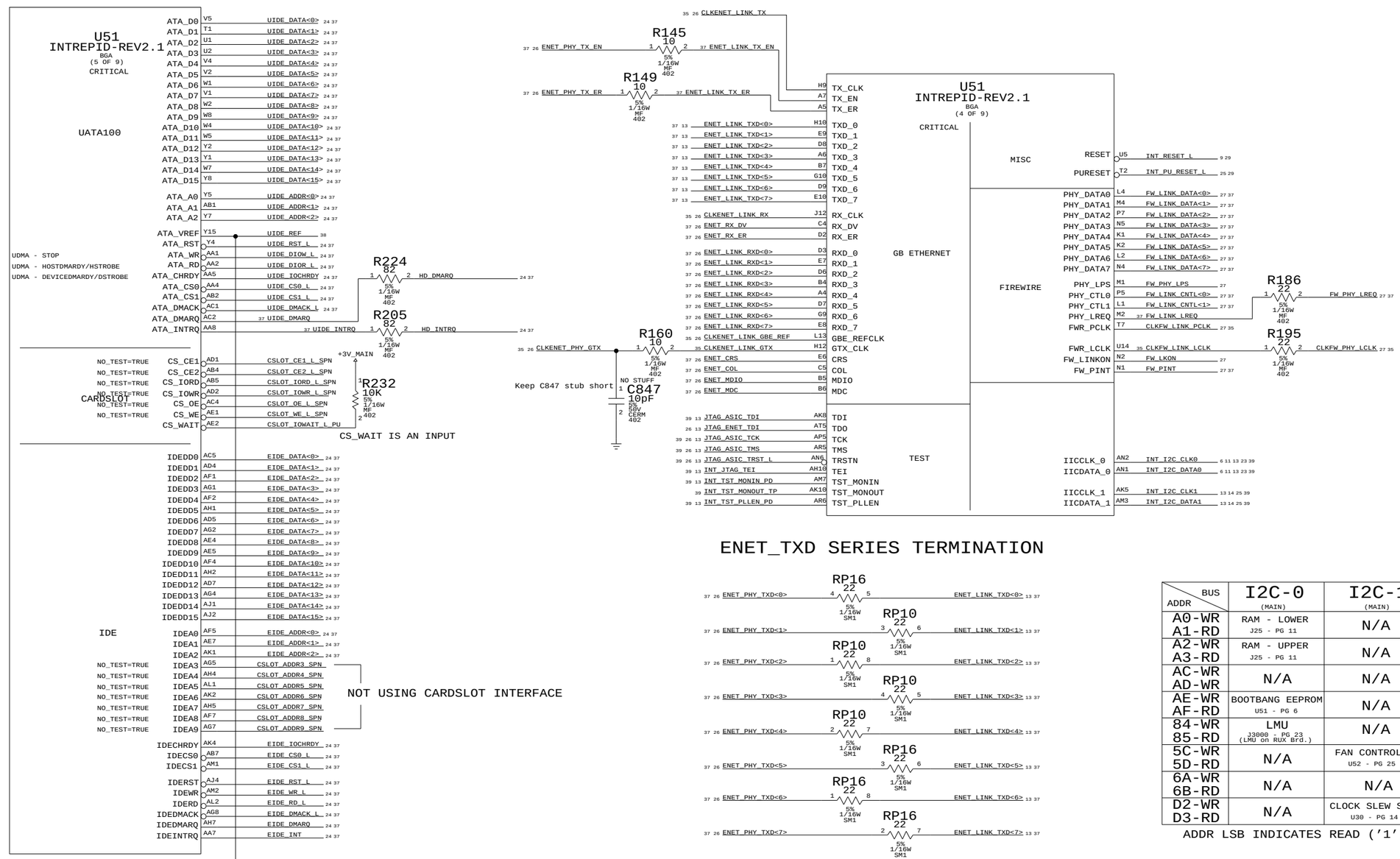

ADDR \ BUS	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - LOWER J25 - PG 11	N/A	N/A	N/A
A2-WR A3-RD	RAM - UPPER J25 - PG 11	N/A	N/A	N/A
AC-WR AD-WR	N/A	N/A	DASH MODEM J14 - PG 25	N/A
AE-WR AF-RD	BOOTBANG EEPROM U51 - PG 6	N/A	N/A	N/A
84-WR 85-RD	LMU J3000 - PG 23 (LMU on RUX Brd.)	N/A	N/A	N/A
5C-WR 5D-RD	N/A	FAN CONTROLLER U52 - PG 25	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J2 - PG 25	N/A
D2-WR D3-RD	N/A	CLOCK SLEW SSCG U30 - PG 14	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

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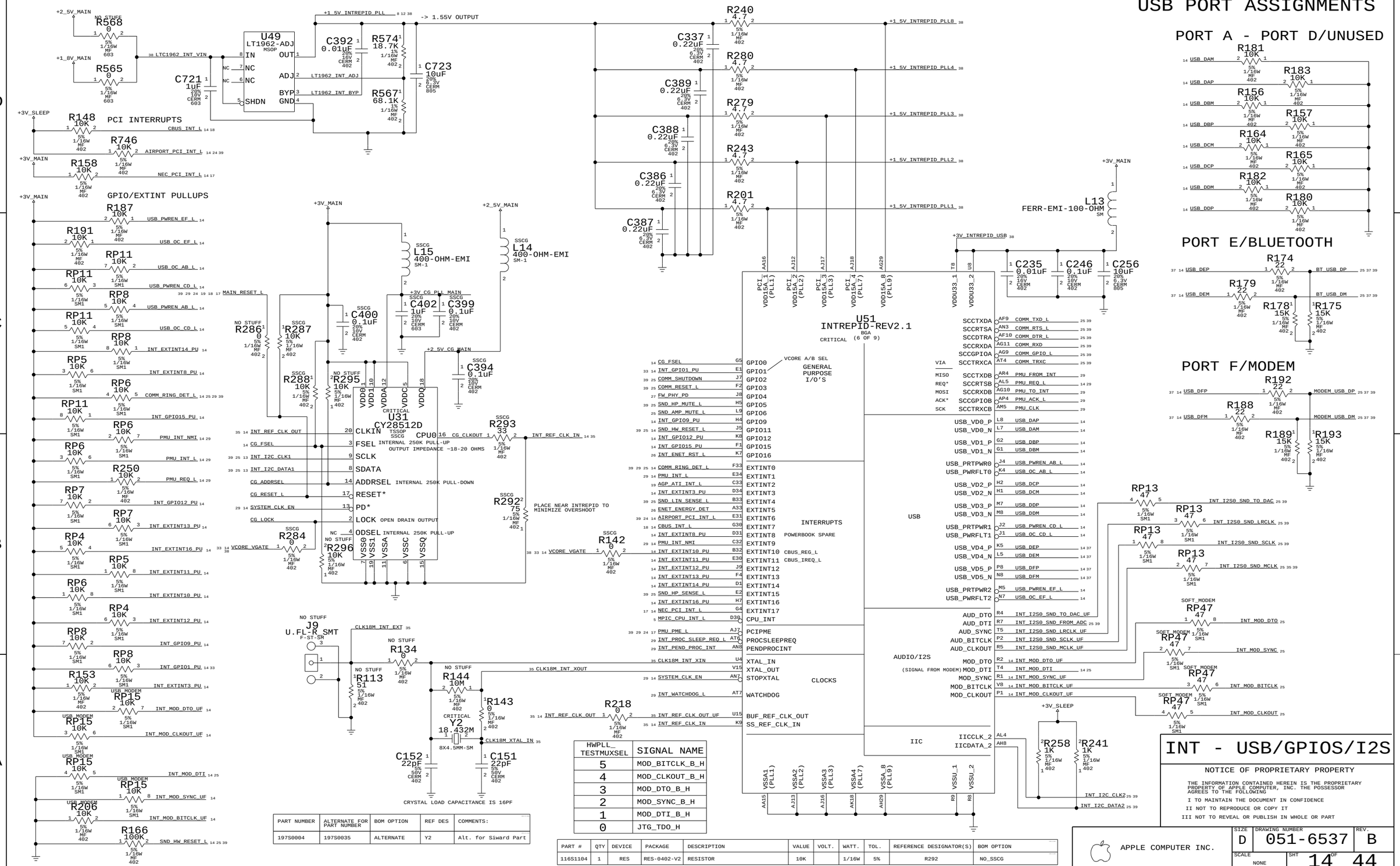
D	051-6537	B
SCALE NONE	SHT 13 OF 44	

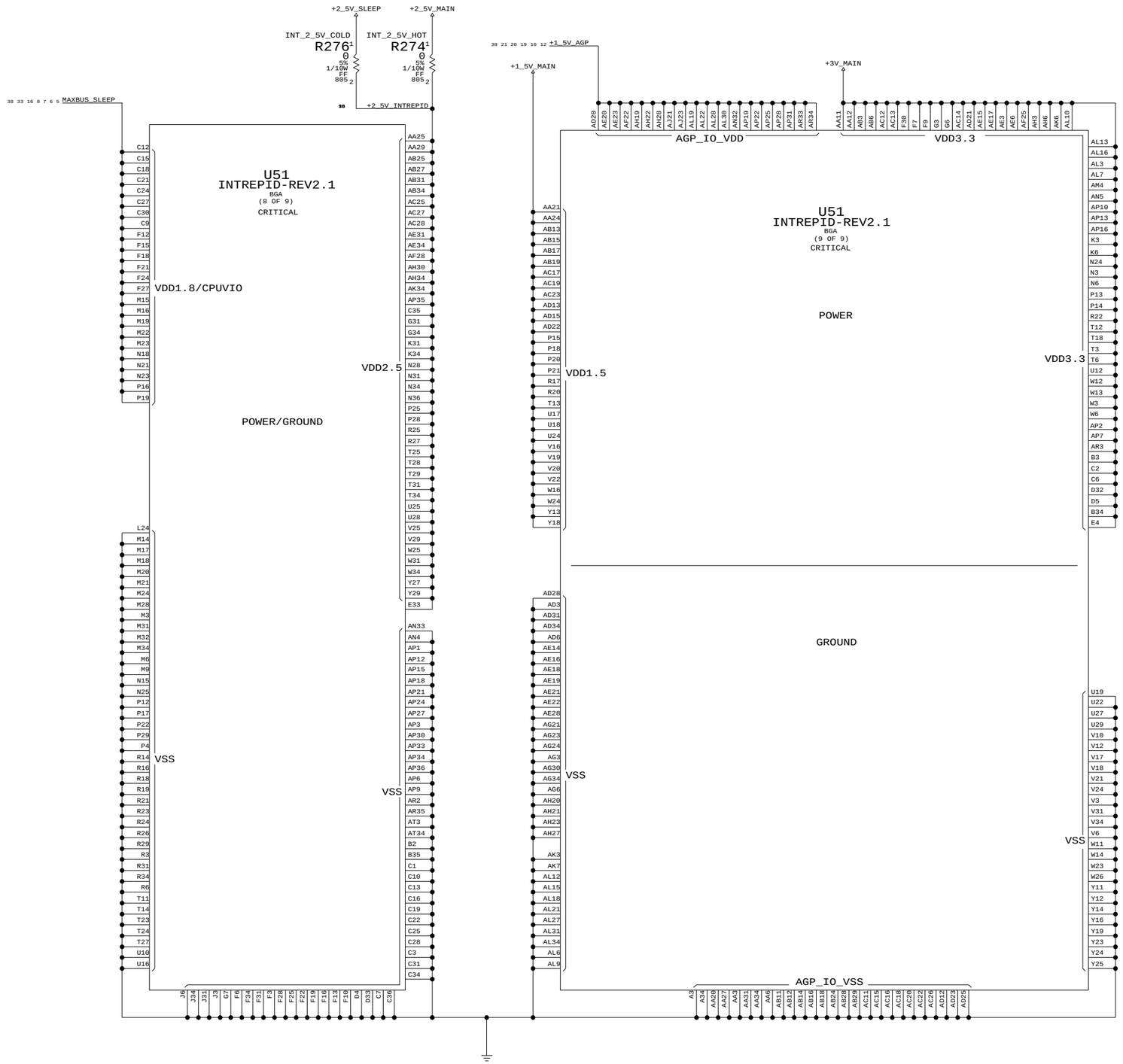
USB PORT ASSIGNMENTS



HWPLL_ TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035	ALTERNATE	Y2	Alt. for Siward Part

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG



Intrepid Power

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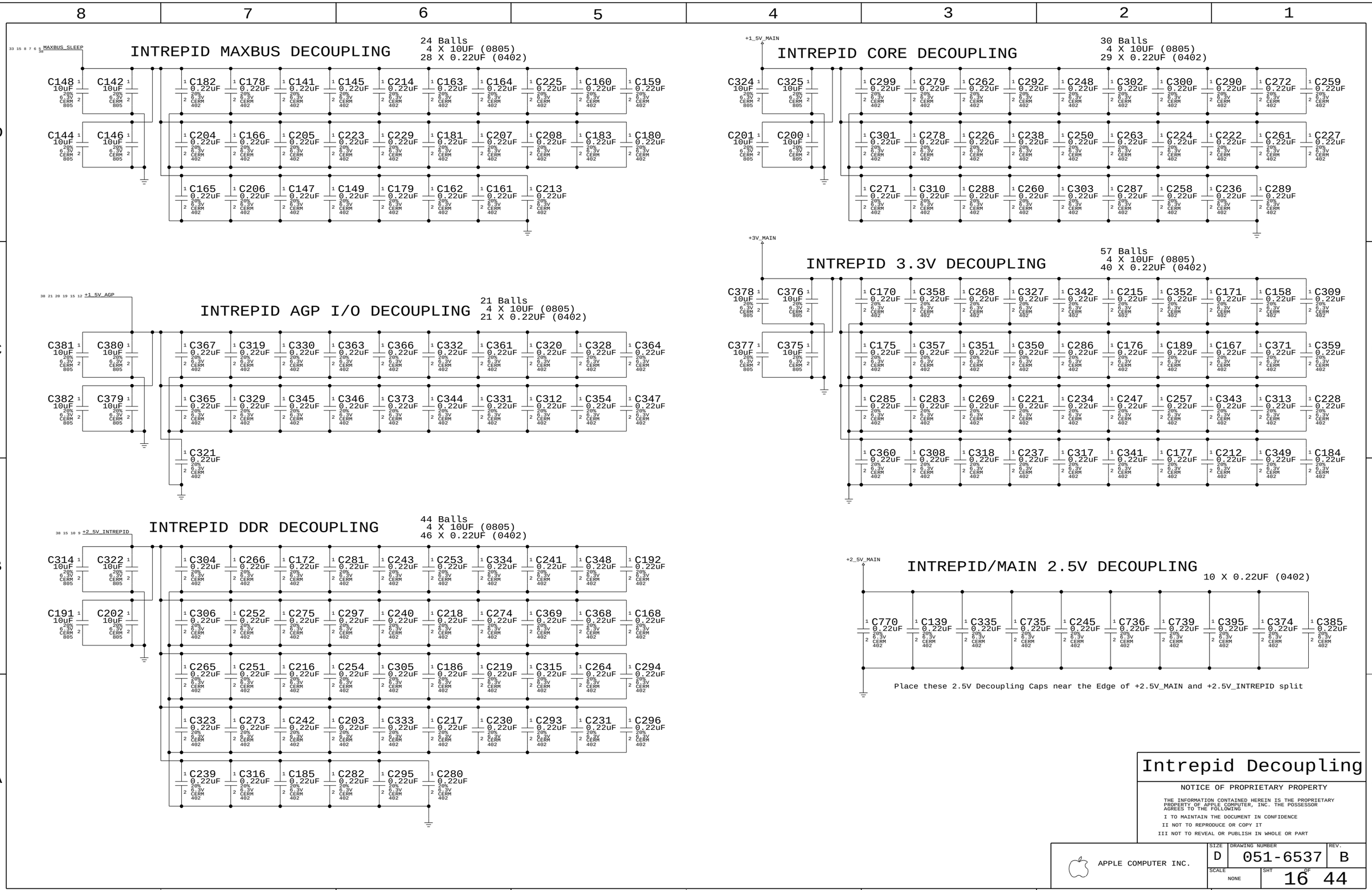
D	051-6537	B
SCALE NONE	SHT 15 OF 44	



Intrepid Decoupling

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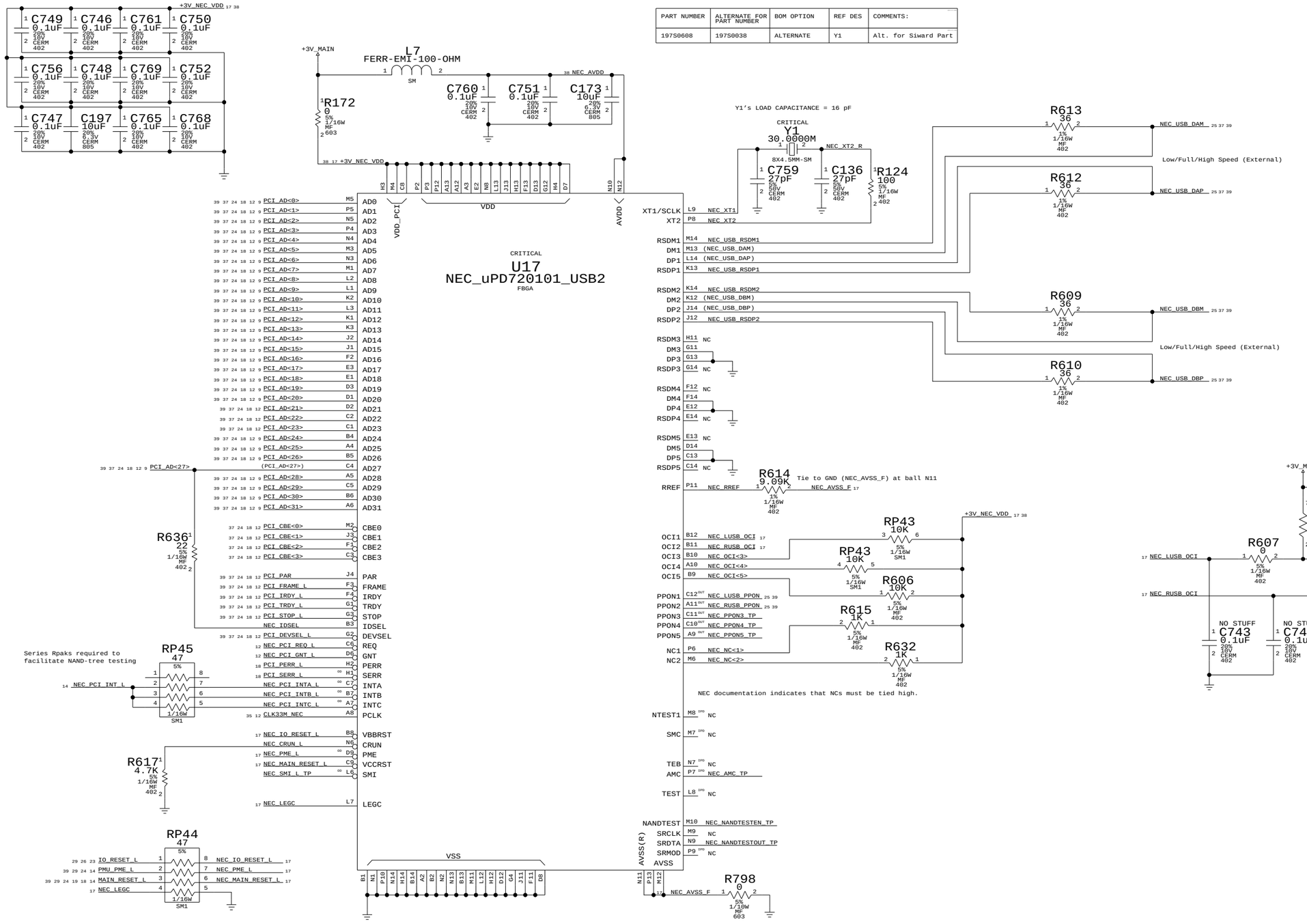
SIZE	DRAWING NUMBER	REV.
D	051-6537	B
SCALE NONE	SHT 16 OF 44	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	ALTERNATE	Y1	Alt. for Siward Part



USB 2.0

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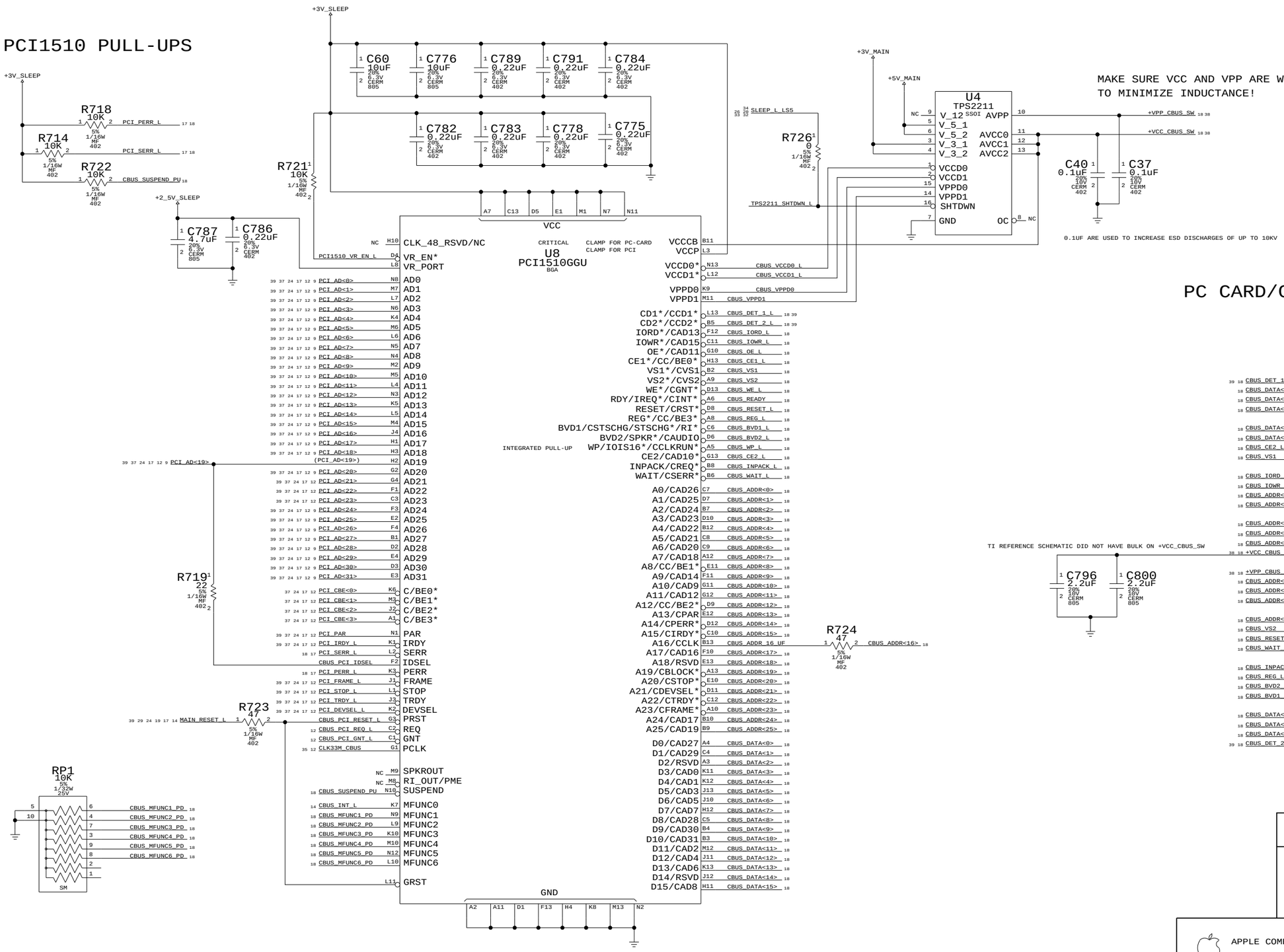
D	051-6537	B
SCALE NONE	SHT 17 OF 44	

PCI1510 PULL-UPS



MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

PC CARD/CARDBUS CONNECTOR

CARDBUS

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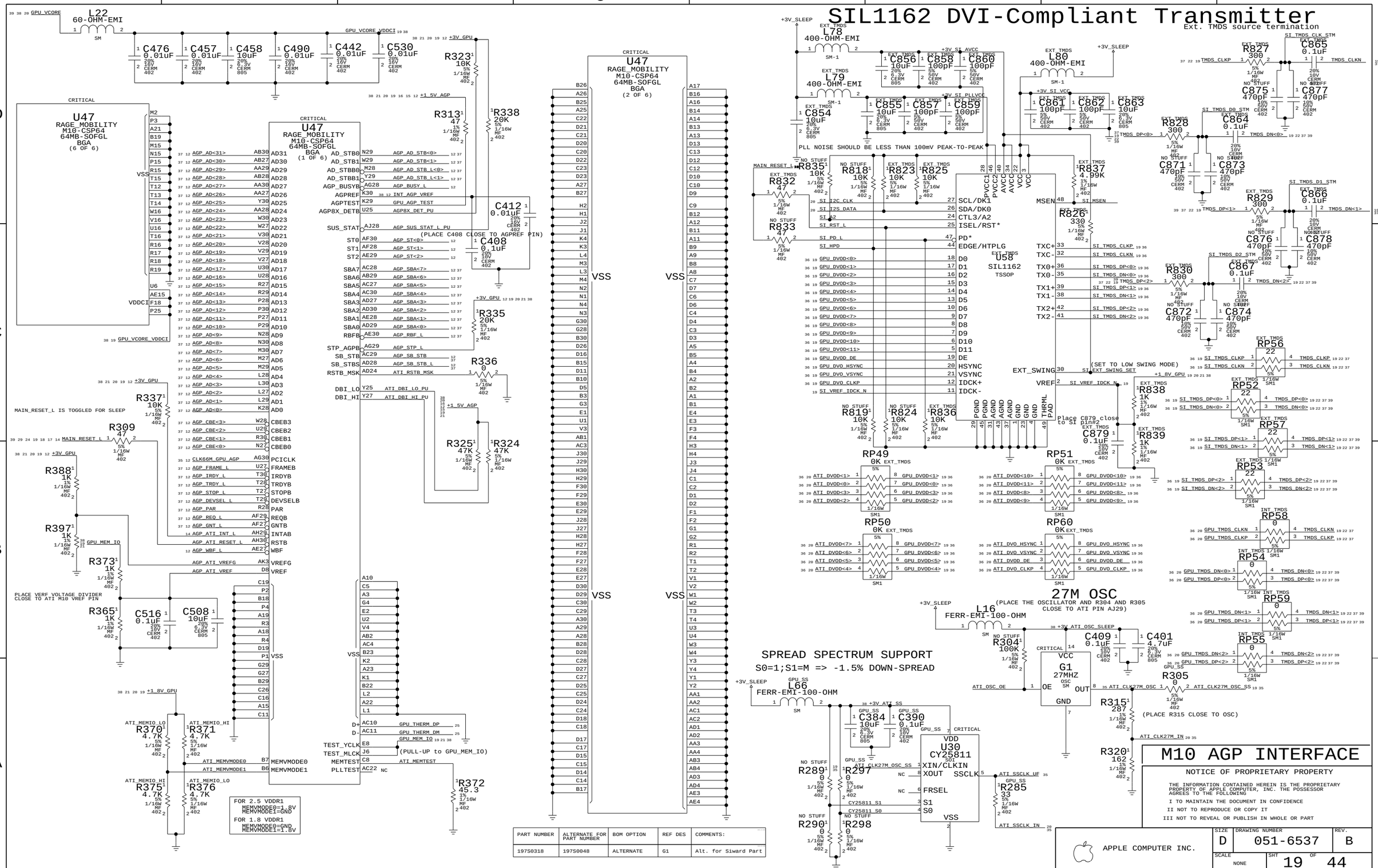
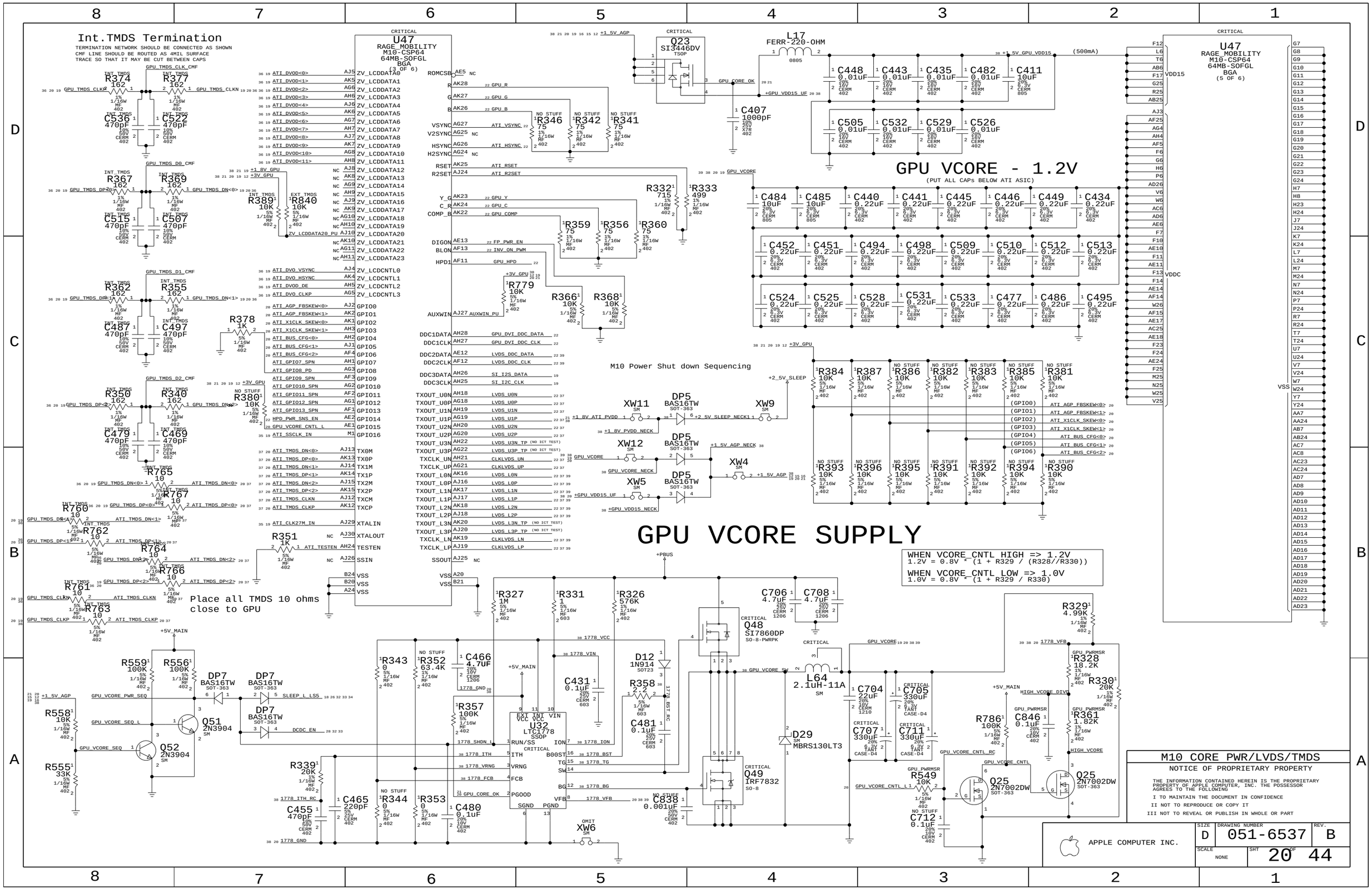
SCALE NONE	SHT 18 OF 44	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0318	197S0048	ALTERNATE	G1	Alt. for Siward Part


Int.TMDS Termination
TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS
U47
RAGE_MOBILITY
M10-CSP64
64MB-SOFGL
BGA
(3 OF 6)
(5 OF 6)
Q23
SI3446DV
TSOP
L17
FERR-220-OHM
0805
(500mA)
GPU VCORE - 1.2V
(PUT ALL CAPs BELOW ATI ASIC)
M10 Power Shut down Sequencing
GPU VCORE SUPPLY
WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R329 / (R328//R330))
WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R329 / R330)
Place all TMDS 10 ohms
close to GPU
Q48
SI7860DP
SO-8-PWRPK
Q49
IRF7832
SO-8
U32
LTC1778
SSOP
L64
2.1uH-11A
SM
D29
MBRS130LT3
Q51
2N3904
Q52
2N3904
Q25
2N7002DW
SOT-363
M10 CORE PWR/LVDS/TMDS
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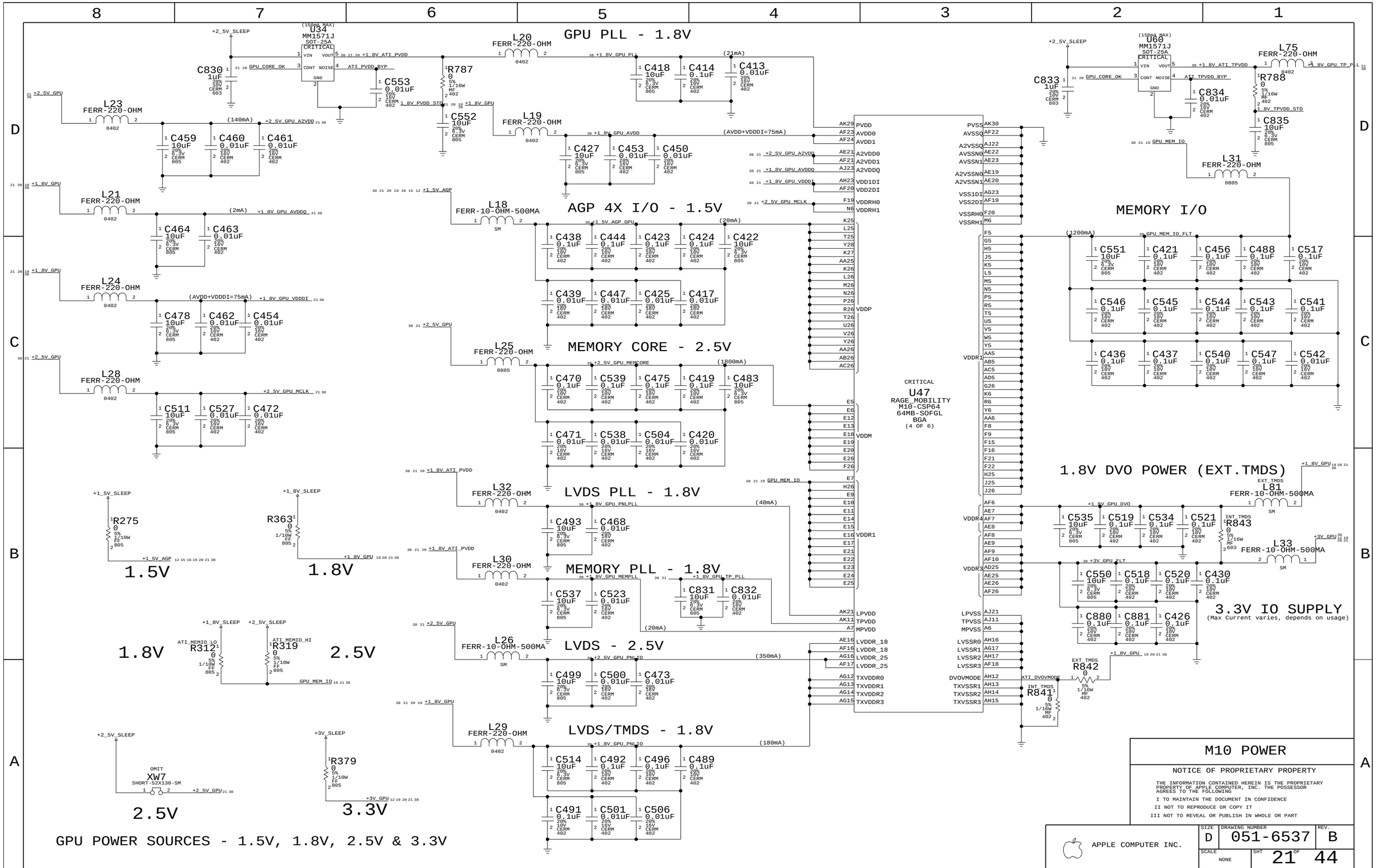
SIZE D
DRAWING NUMBER 051-6537
REV. B
SCALE NONE
SHT 20 OF 44


GPU PLL - 1.8V
AGP 4X I/O - 1.5V
MEMORY CORE - 2.5V
LVDS PLL - 1.8V
MEMORY PLL - 1.8V
LVDS - 2.5V
LVDS/TMDS - 1.8V
MEMORY I/O
1.8V DVO POWER (EXT.TMDS)
3.3V IO SUPPLY
(Max Current varies, depends on usage)
U47
RAGE MOBILITY
M10-CSP64
64MB-SOFGL
BGA
(4 OF 6)
U34
MM1571J
SOT-25A
U60
MM1571J
SOT-25A
1.5V
1.8V
1.8V
2.5V
2.5V
3.3V
GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V
M10 POWER
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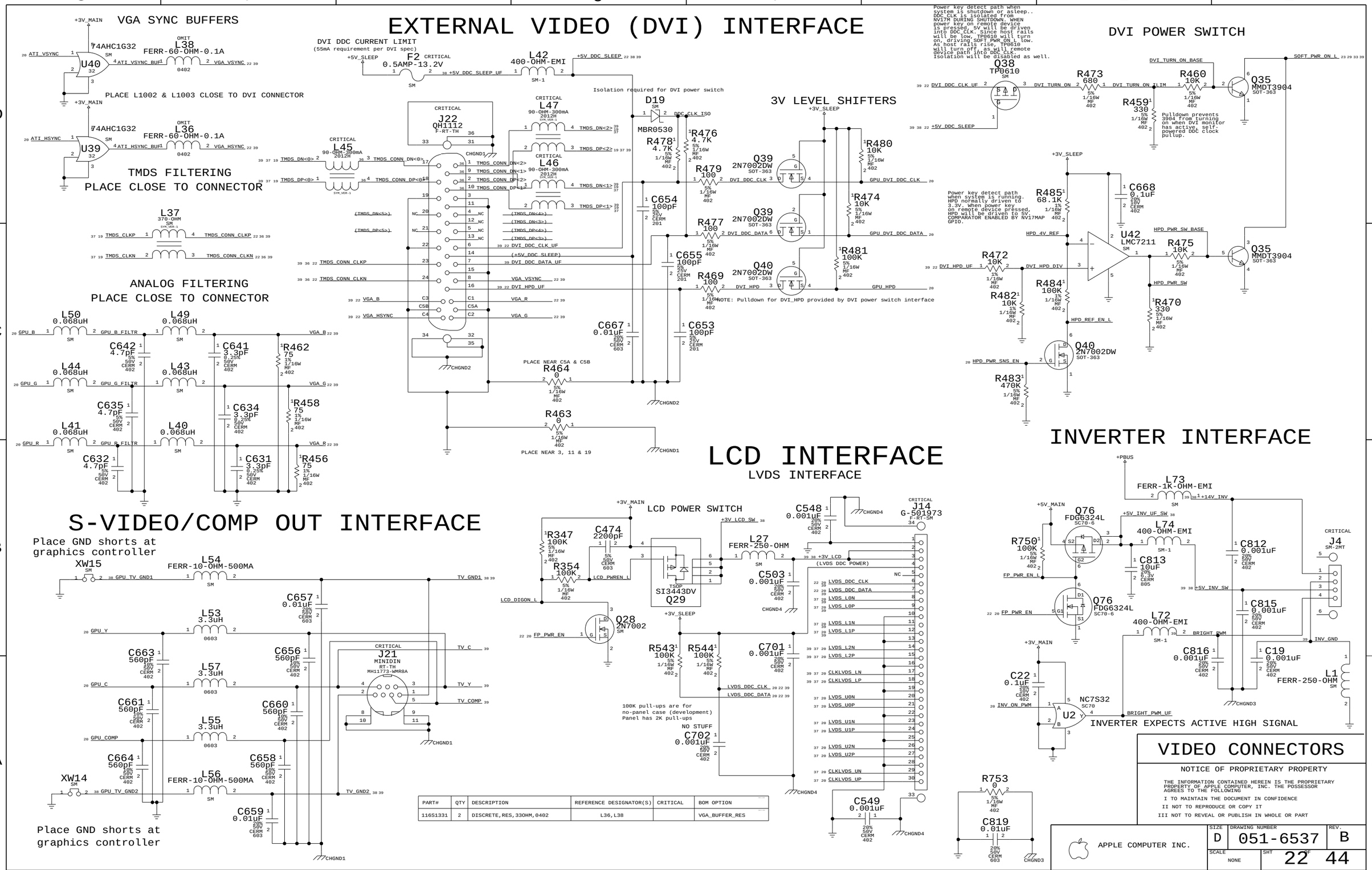
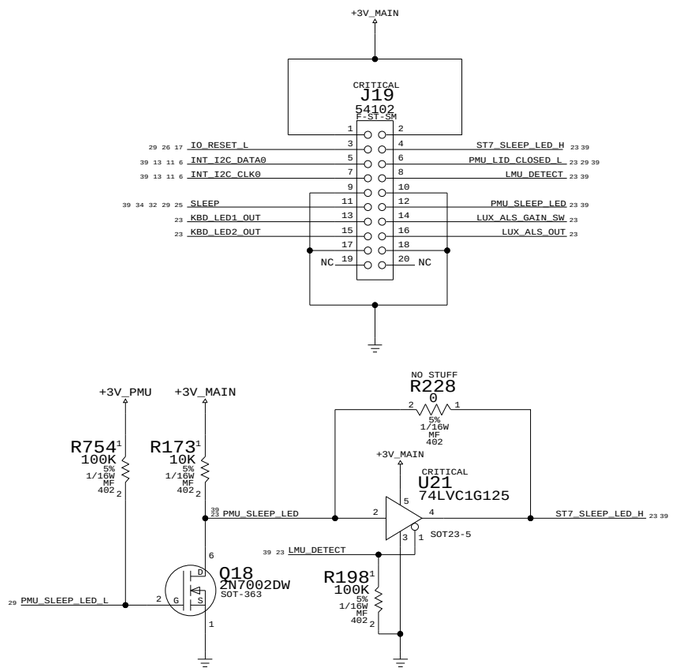
SIZE D
DRAWING NUMBER 051-6537
REV. B
SCALE NONE
SHT 21 OF 44

EXTERNAL VIDEO (DVI) INTERFACE

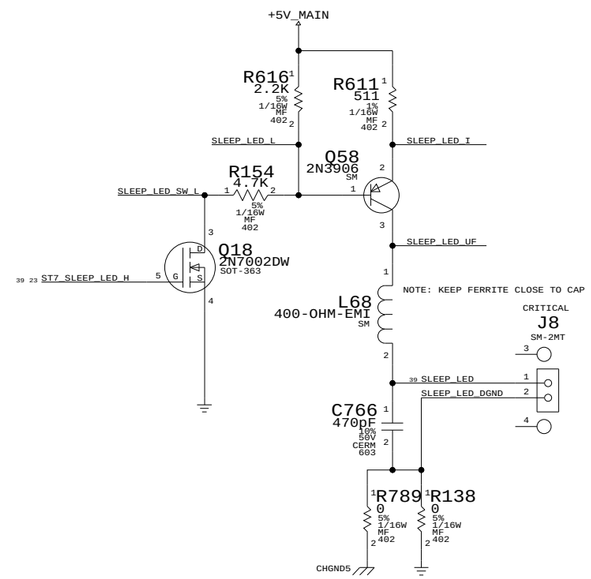


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE,RES,330HM,0402	L36,L38		VGA_BUFFER_RES

LMU/RIGHT SENSOR CONNECTOR

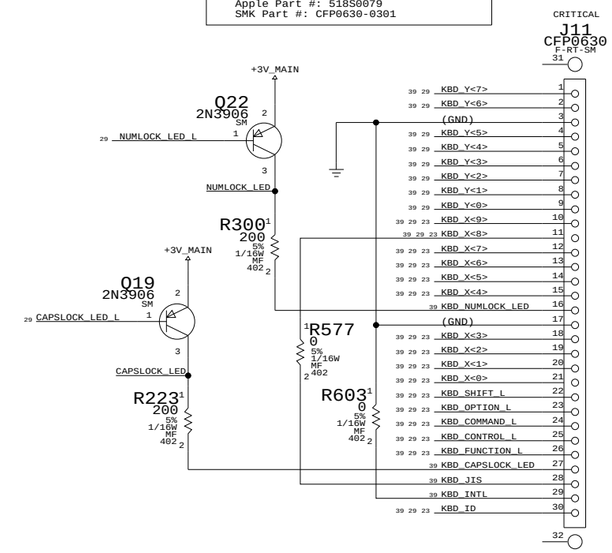


SLEEP LED

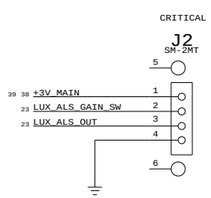


TOP CONTACT ZIF KEYBOARD CONN

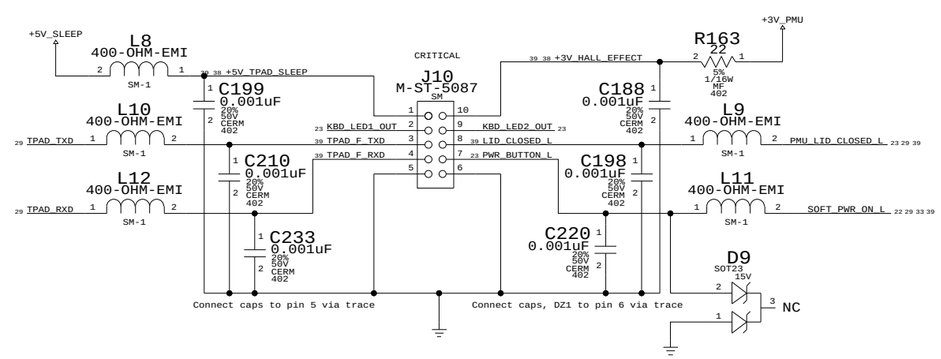
CONN,TOP CONTACT ZIF,0.8MM PITCH,30P,SM
Apple Part #: 518S0079
SMK Part #: CFP0630-0301



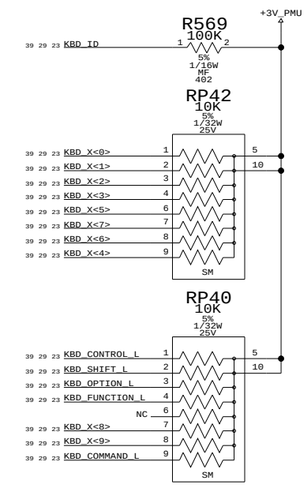
LEFT LIGHT SENSOR CONNECTOR



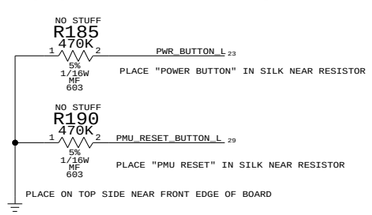
TRACKPAD/PWR BTN CONN



KEYBOARD PULLUPS



DEBUG HELPERS



KEYBOARD/TPAD/SLEEP LED

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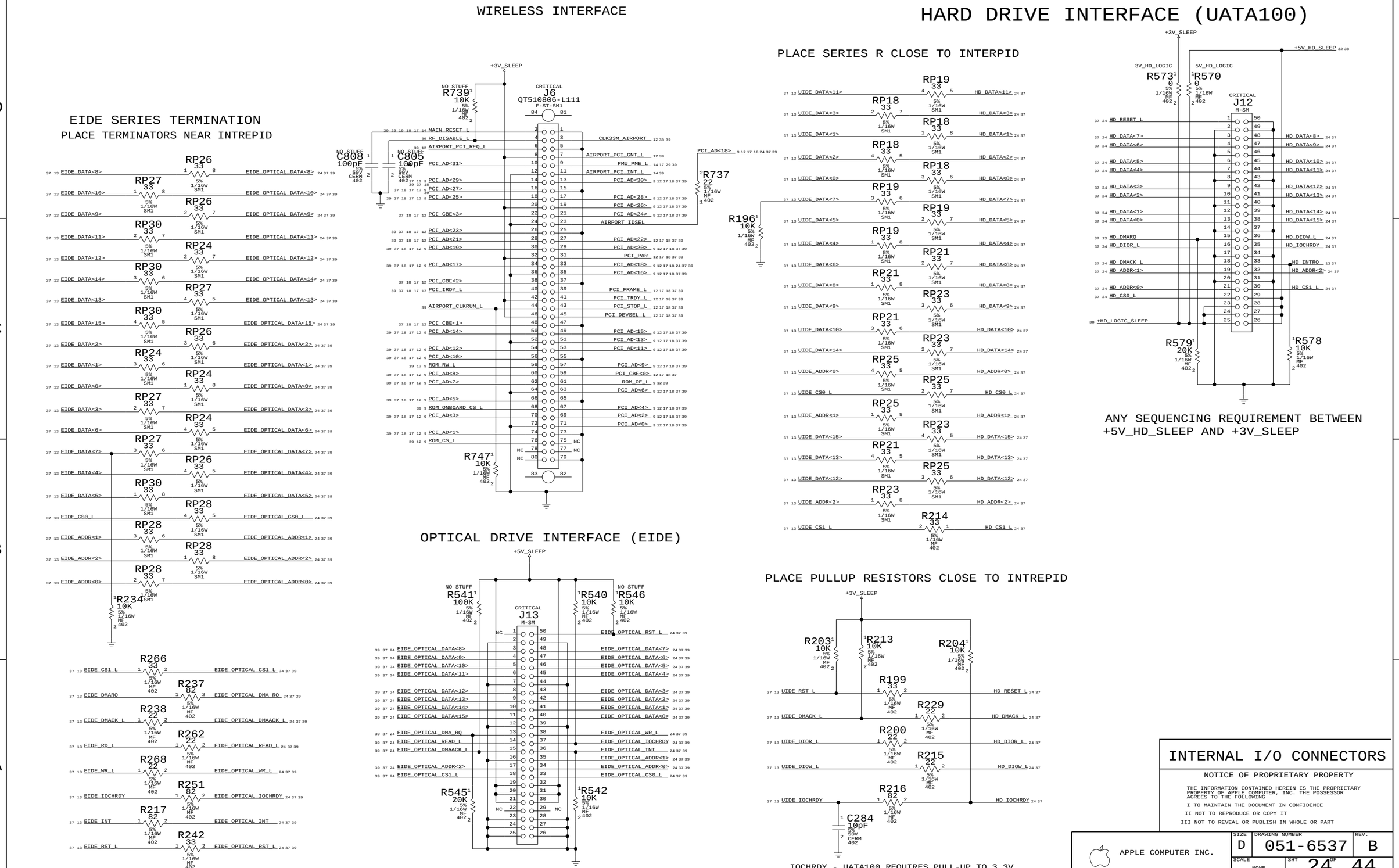
SCALE NONE	SHT 23 OF 44	


WIRELESS INTERFACE
HARD DRIVE INTERFACE (UATA100)
EIDE SERIES TERMINATION
PLACE TERMINATORS NEAR INTREPID
PLACE SERIES R CLOSE TO INTERPID
OPTICAL DRIVE INTERFACE (EIDE)
PLACE PULLUP RESISTORS CLOSE TO INTREPID
ANY SEQUENCING REQUIREMENT BETWEEN
+5V_HD_SLEEP AND +3V_SLEEP
IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V
INTERNAL I/O CONNECTORS
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SIZE D
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REV. B
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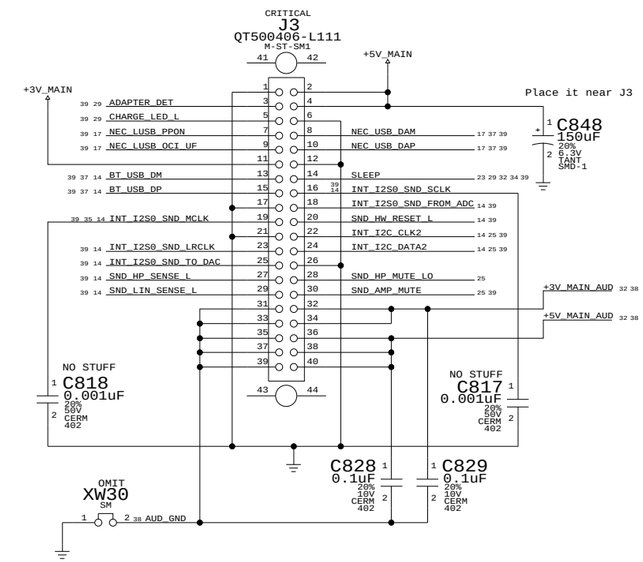
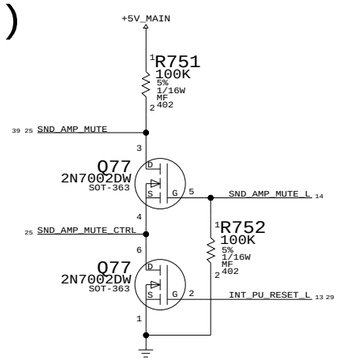
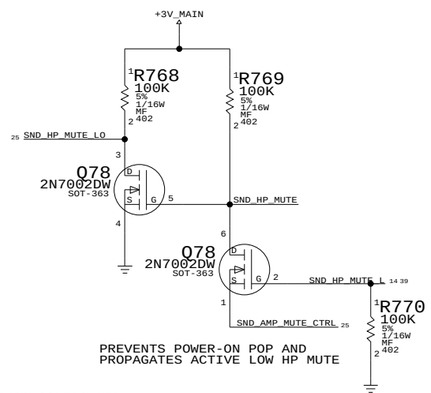
LEFT I/O & AUDIO BOARD (LIO)



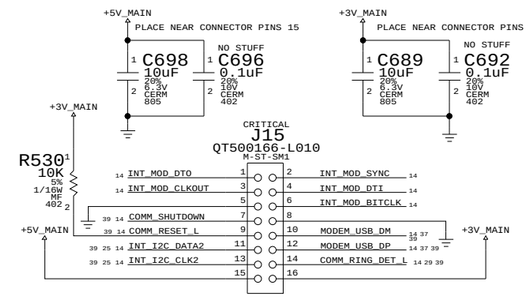


PREVENTS POWER-ON POP AND
GENERATES ACTIVE HIGH SPKR MUTE



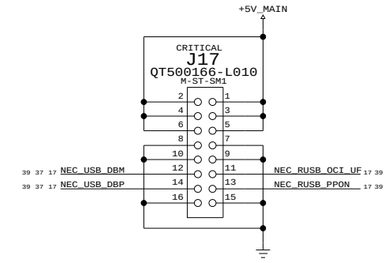
PREVENTS POWER-ON POP AND
PROPAGATES ACTIVE LOW HP MUTE

USB MODEM/SOFT MODEM

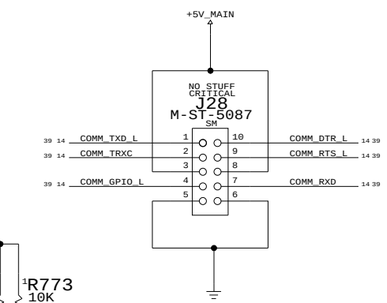


MODEM I2C ADDR ASSIGNED VIA FLEX CABLE

RIGHT USB BOARD

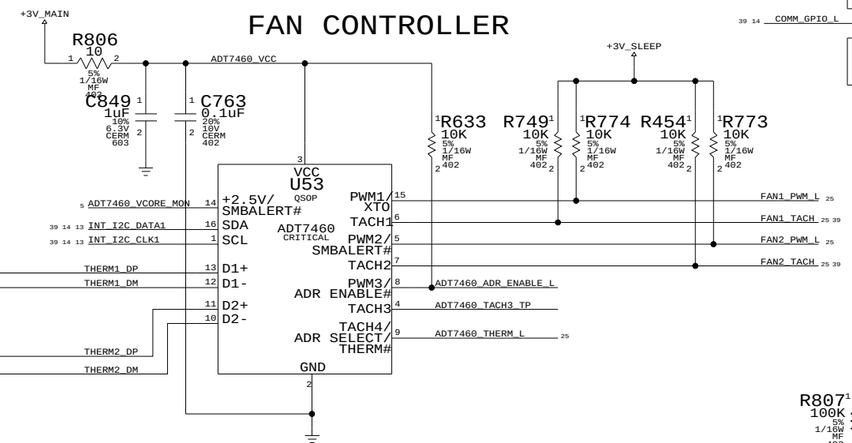


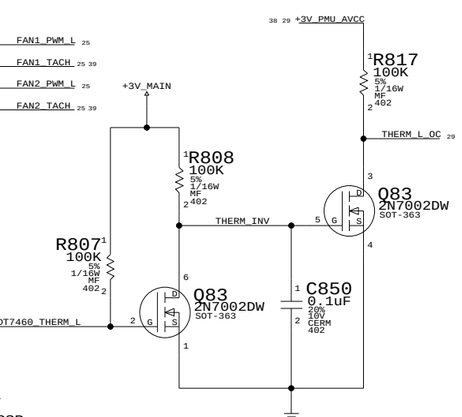
SERIAL DEBUG INTERFACE



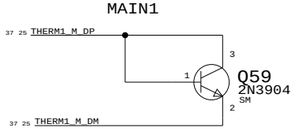
FAN INTERFACE

FAN CONTROLLER

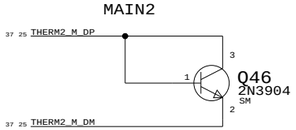




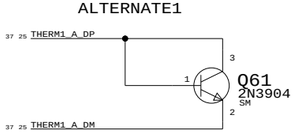
PLACE CLOSE TO CPU
MAIN1



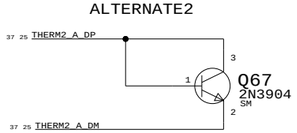
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2



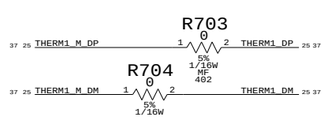
PLACE UNDERNEATH UPPER RAM
ALTERNATE1

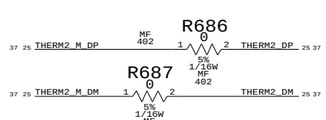


PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2

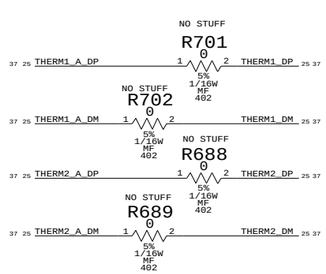


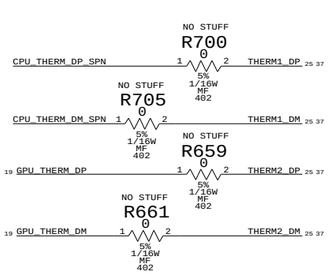
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



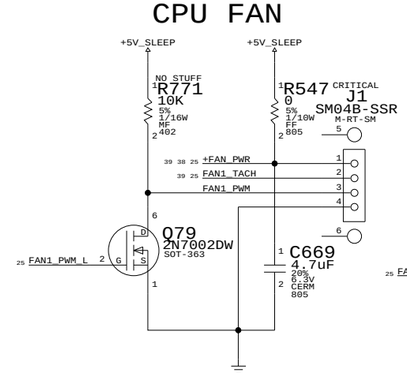


KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

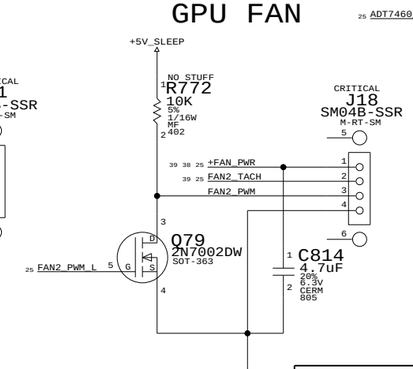




CPU FAN



GPU FAN



FAN/MODEM/SOUND/BACKUP BATT.

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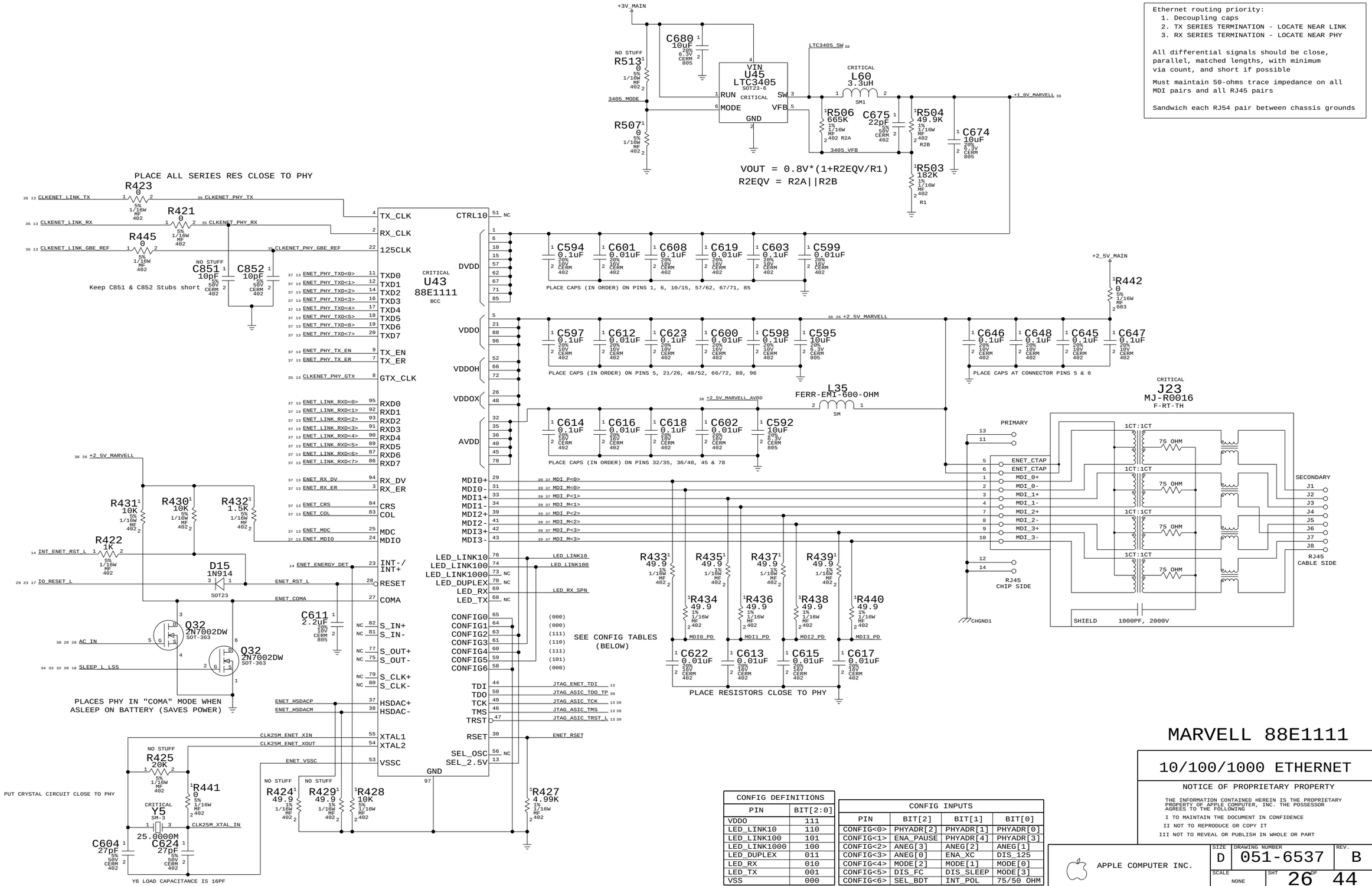
Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds



CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

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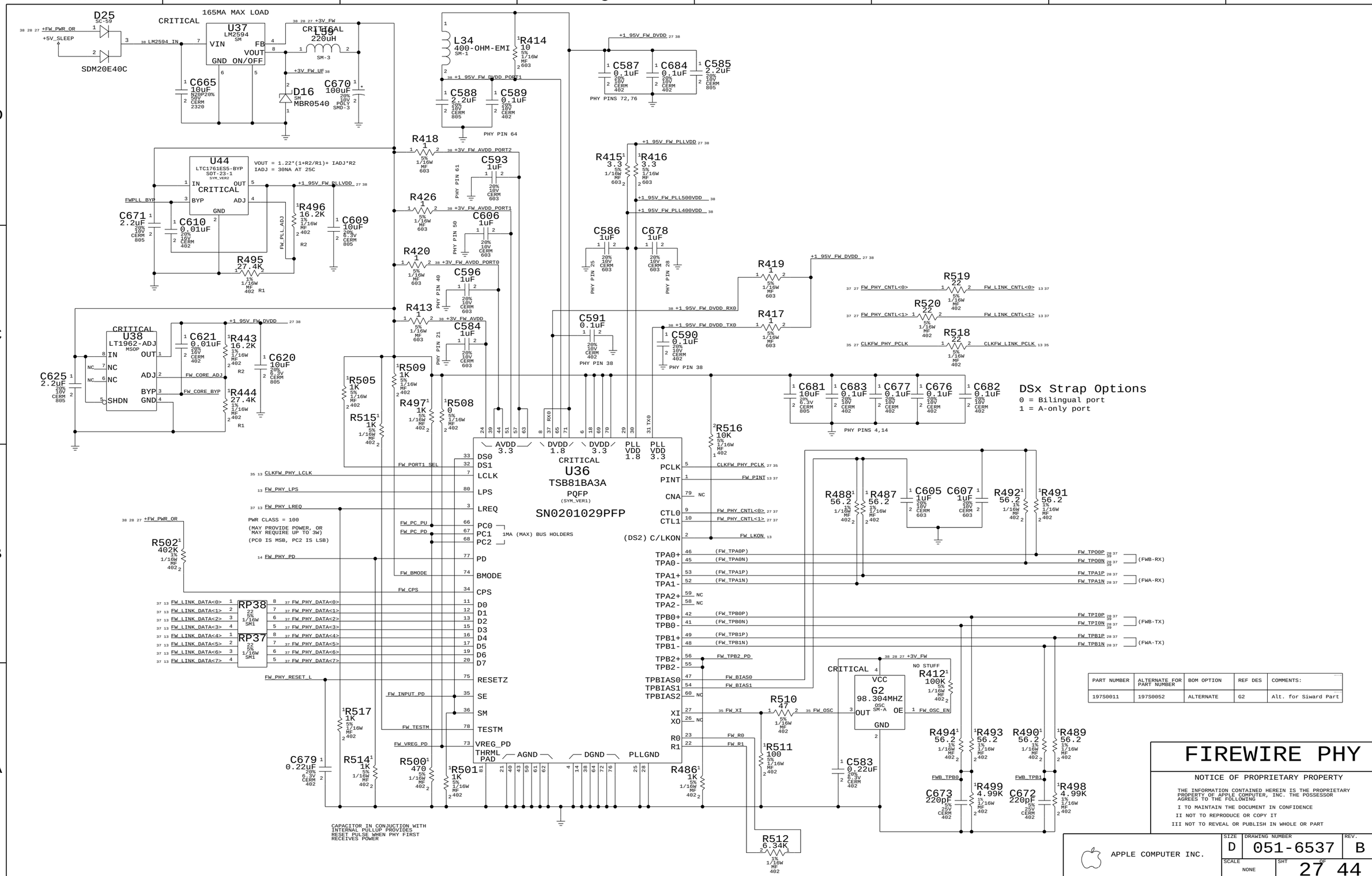

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052	ALTERNATE	G2	Alt. for Siward Part

FIREWIRE PHY

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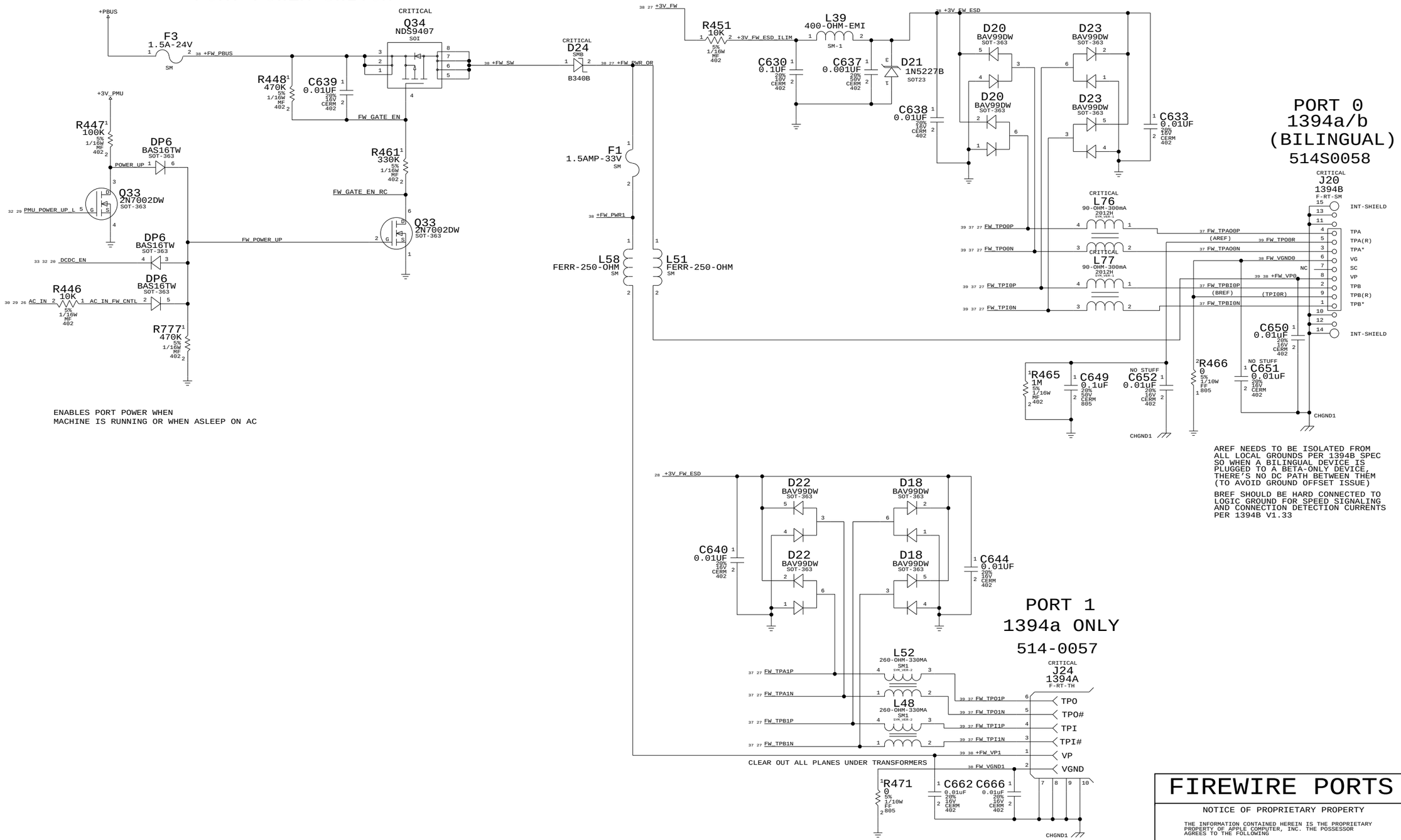
PORT POWER SWITCH



FIREWIRE PORTS

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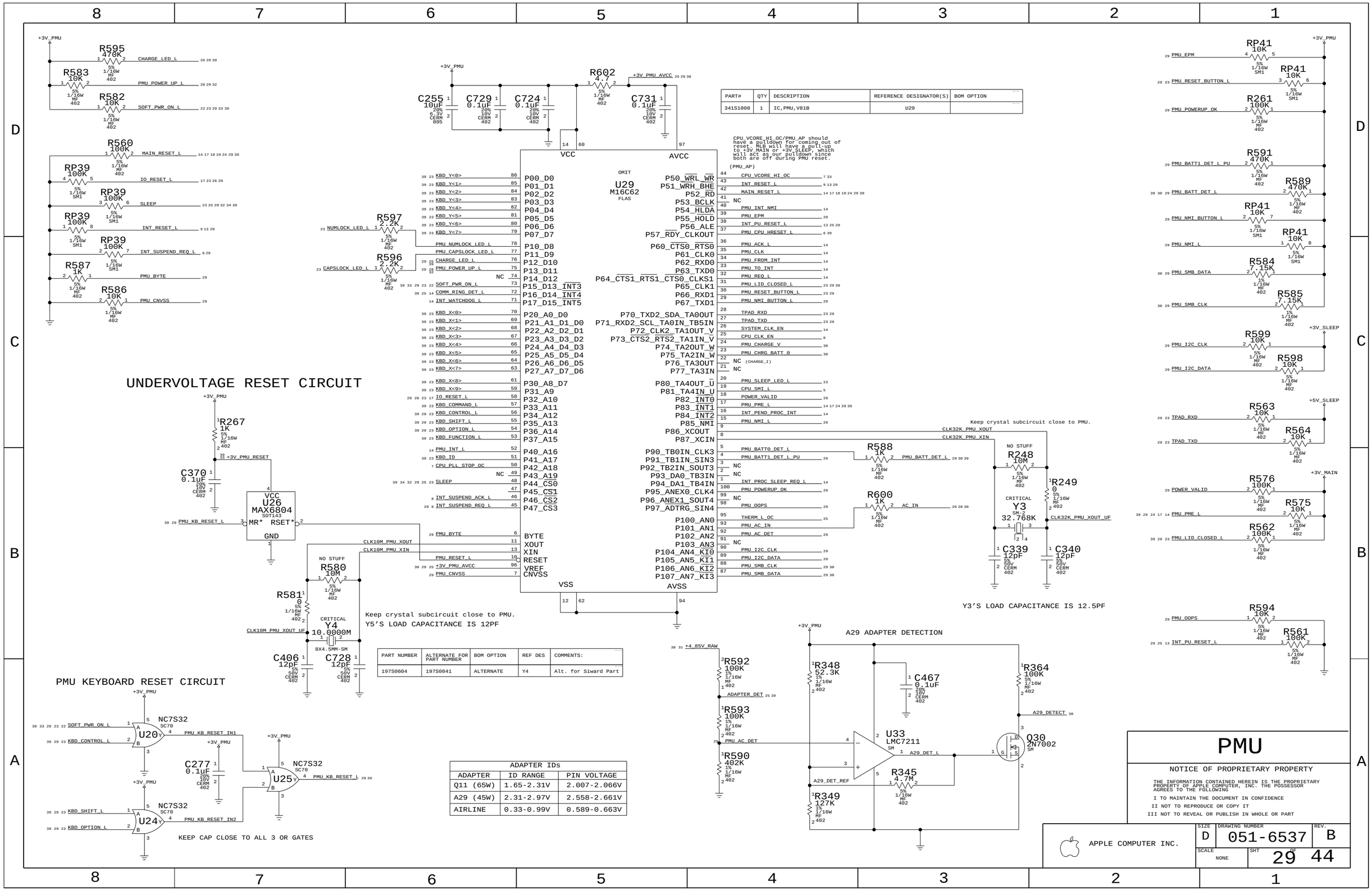
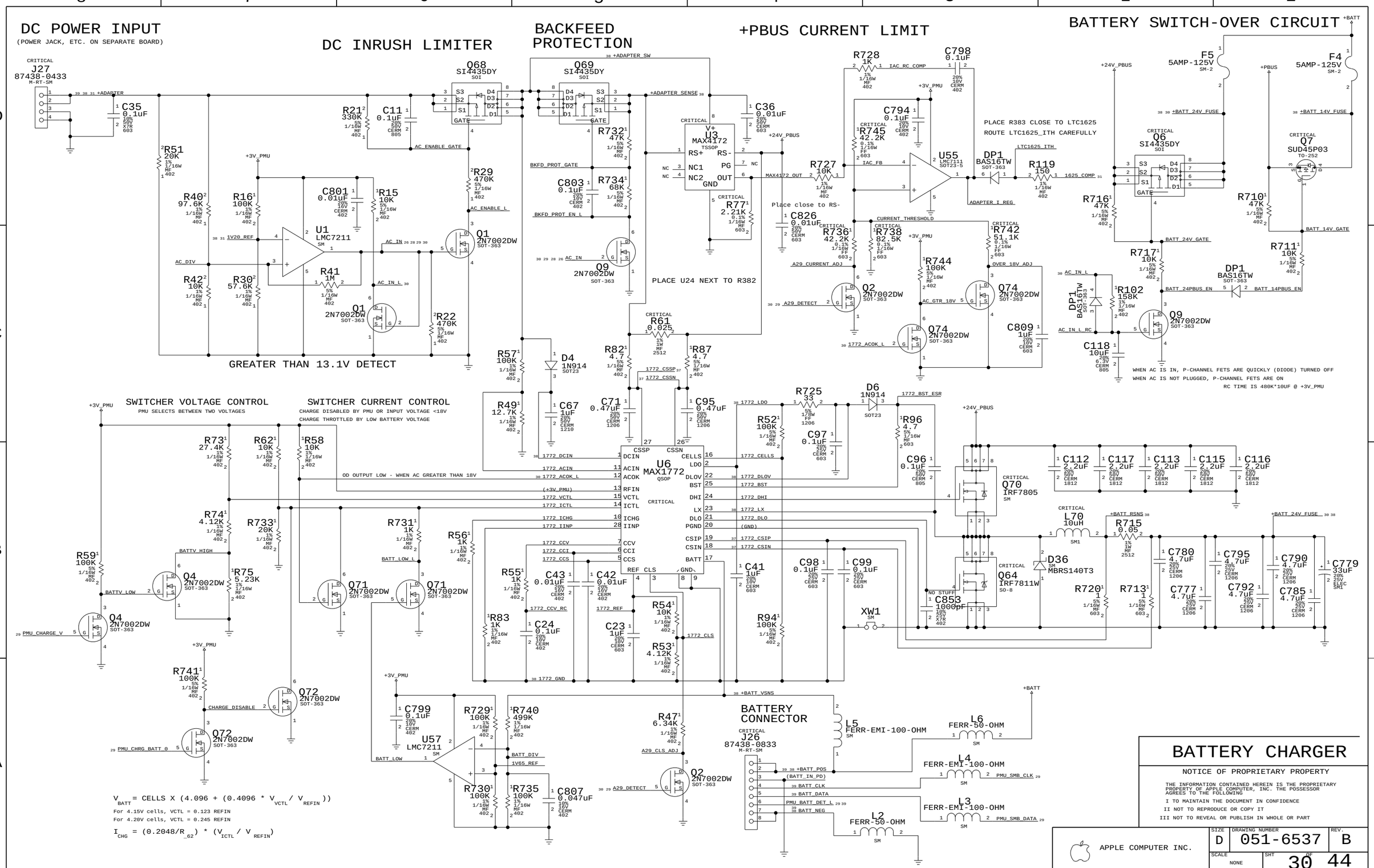


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U29	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0604	197S0041	ALTERNATE	Y4	Alt. for Siward Part

ADAPTER IDs		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V



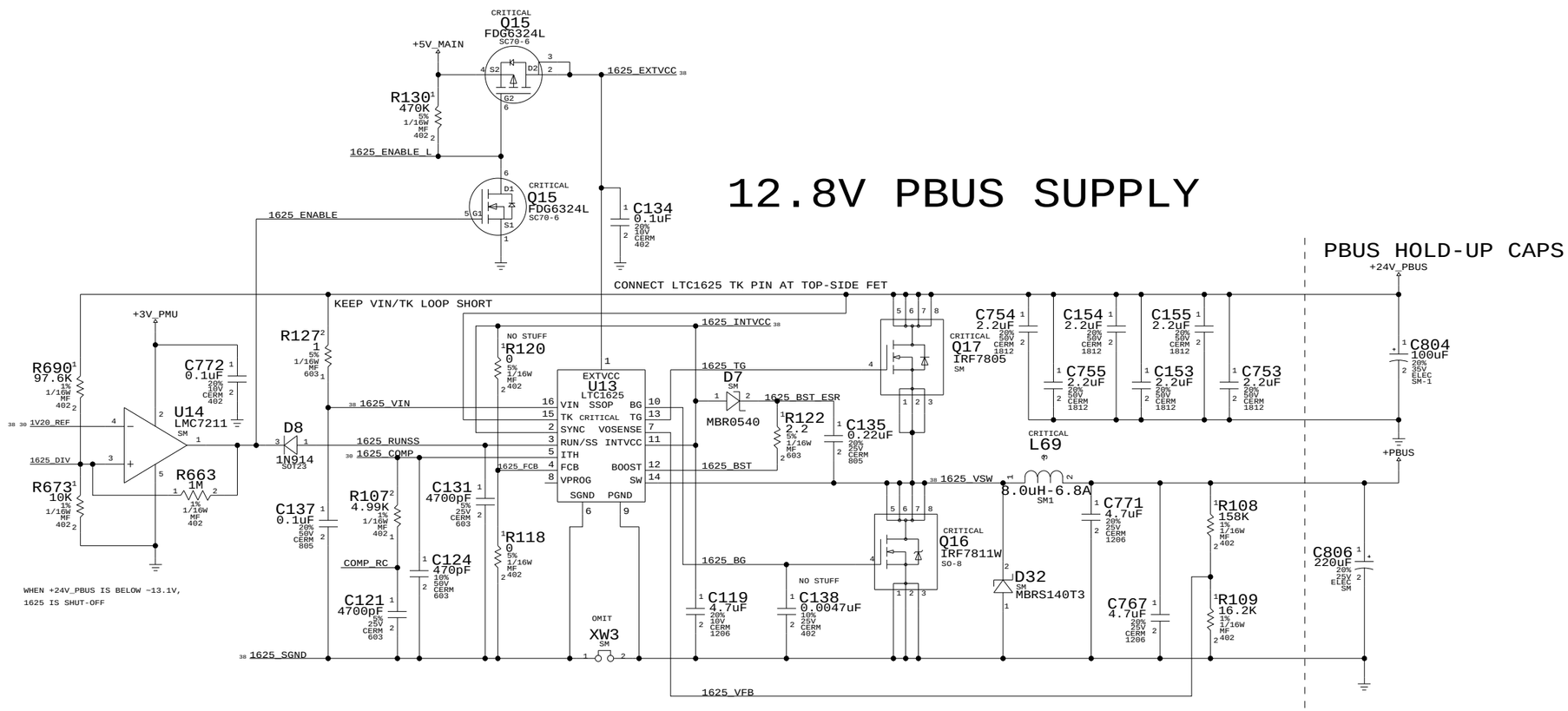
$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

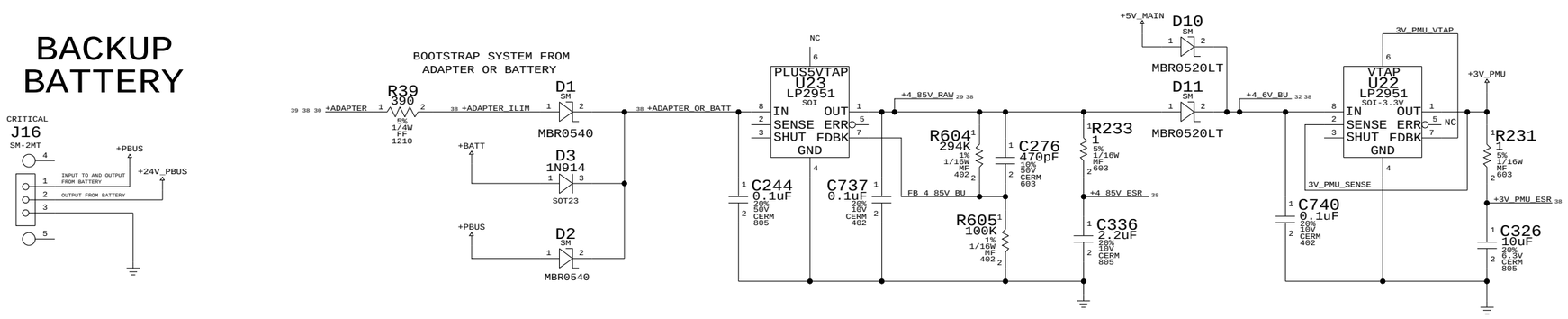
For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

12.8V PBUS SUPPLY



PMU SUPPLY



12.8V REGULATOR

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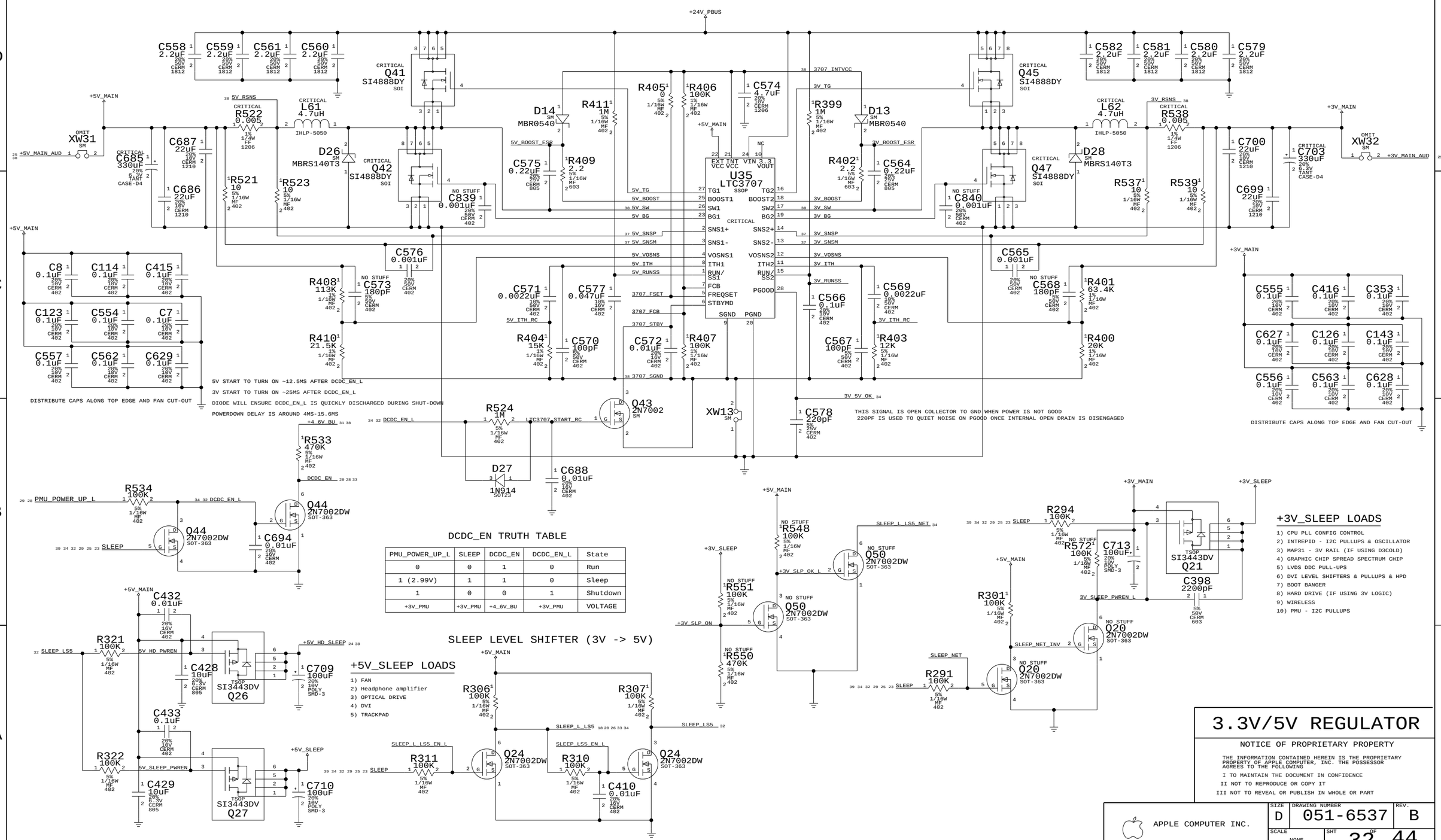
3.3V/5V MAIN SUPPLY



PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

DCDC_EN TRUTH TABLE

3.3V/5V REGULATOR

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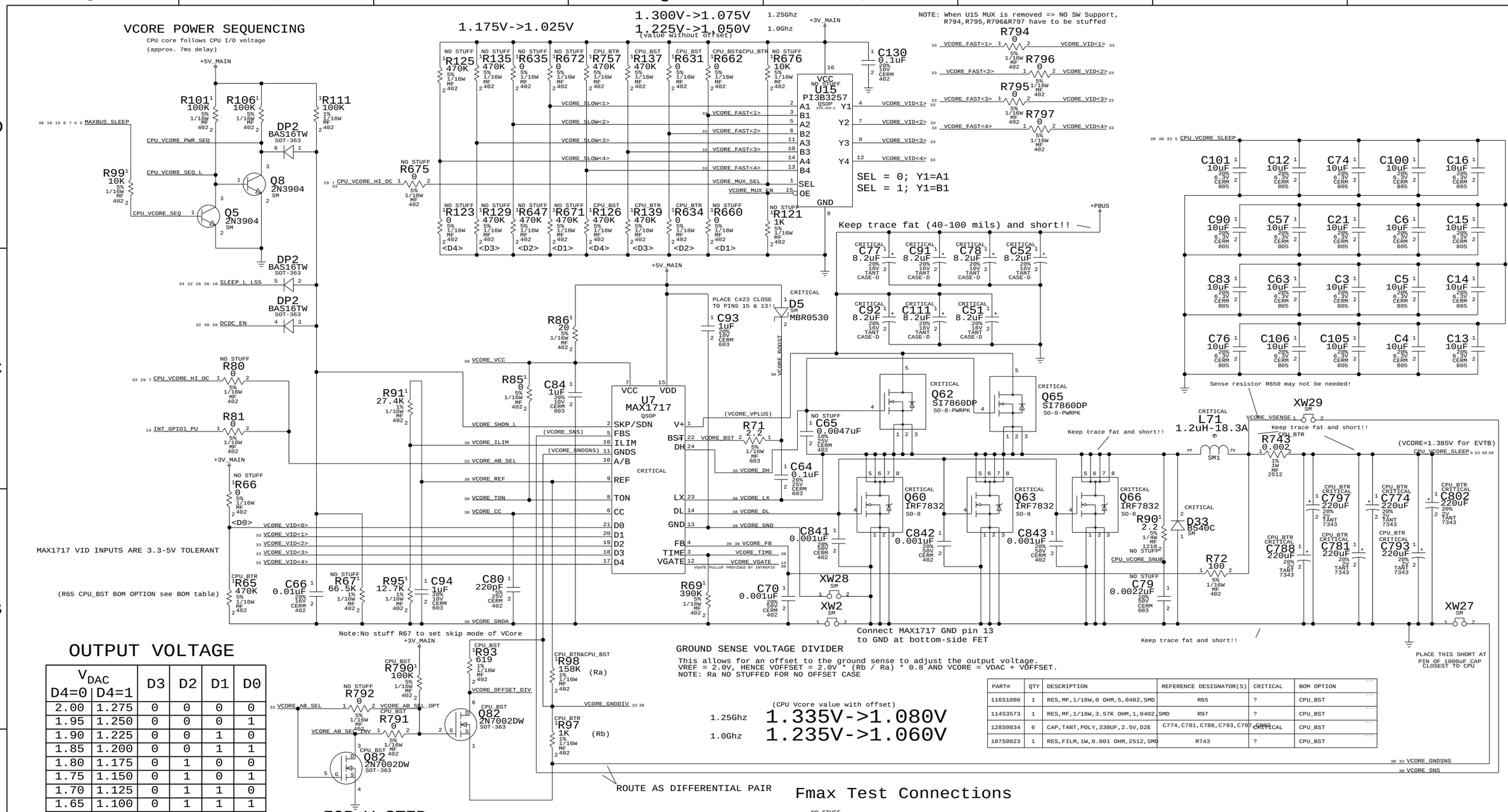

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1
If all pull-ups are >=100K and all
pull-downs are <=1K, $V_A = V_B$.

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * (Rb / Ra) * 0.8 AND VCORE = VDAC + VOFFSET.
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

(CPU Vcore value with offset)

1.25Ghz 1.335V->1.080V

1.0Ghz 1.235V->1.060V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1000	1	RES,MF,1/16W,0 OHM,5,0402,SMD	R65	?	CPU_BST
114S3573	1	RES,MF,1/16W,3.57K OHM,1,0402,SMD	R97	?	CPU_BST
128S0034	6	CAP,TANT,POLY,330UF,2.5V,D2E	C774,C781,C788,C793,C797,C802	CRITICAL	CPU_BST
107S0023	1	RES,FILM,1W,0.001 OHM,2512,SMD	R743	?	CPU_BST

Fmax Test Connections

VCORE SUPPLY

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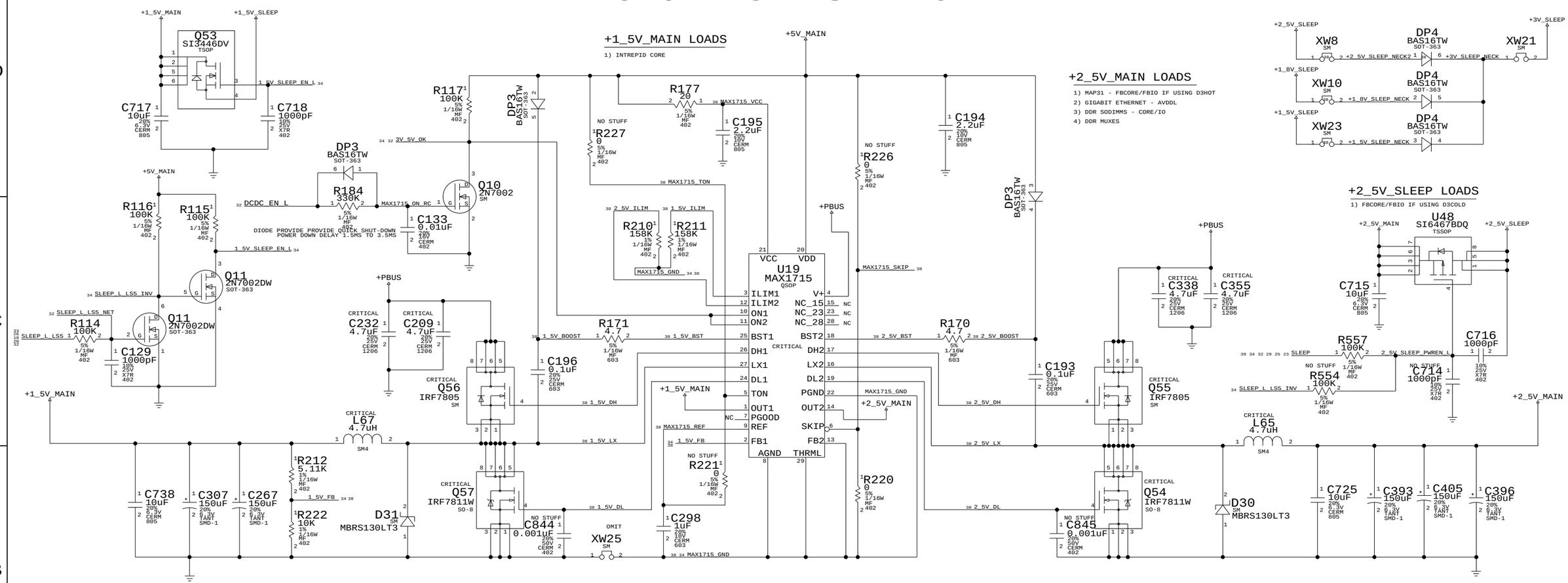
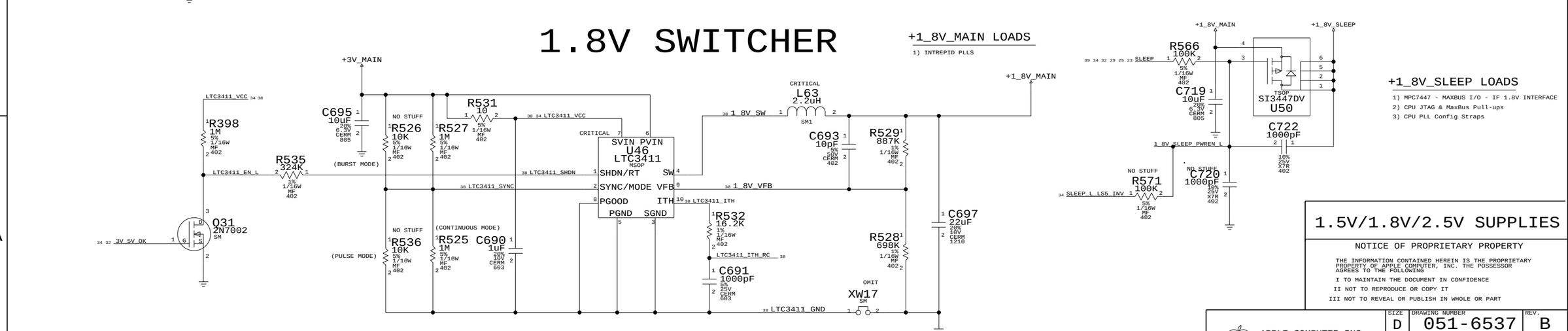
1.5V/2.5V SWITCHER



1.8V SWITCHER



1.5V/1.8V/2.5V SUPPLIES

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DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
				STUB_LENGTH OF 200 MILS NEEDED WHEN WE CONVERT TO 14.2					
GROUP 0	MEM_DATA<7..0>	L:S:1602:1700	7	500	(200)			167 MHZ	9 10
	MEM_DQM<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	MEM_DQS<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	RAM_DATA_A<7..0>	L:S:1903:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ	10 11
	RAM_DQM_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DATA_B<7..0>	L:S:2000:2100	7	500	(200)			167 MHZ	10 11
	RAM_DQM_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
GROUP 1	MEM_DATA<15..8>	L:S:1344:1660	7	500	(200)			167 MHZ	9 10
	MEM_DQM<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	MEM_DQS<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167.0 MHz:::	9 10
	RAM_DATA_A<15..8>	L:S:1905:2000	7	500	(200)			167 MHZ	10 11
	RAM_DQM_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DATA_B<15..8>	L:S:2004:2412	7	500	(200)			167 MHZ	10 11
	RAM_DQM_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
GROUP 2	MEM_DATA<23..16>	L:S:1435:1500	7	500	(200)			167 MHZ	9 10
	MEM_DQM<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	MEM_DQS<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167.0 MHz:::	9 10
	RAM_DATA_A<23..16>	L:S:1707:1800	7	500	(200)			167 MHZ	10 11
	RAM_DQM_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DATA_B<23..16>	L:S:1900:2000	7	500	(200)			167 MHZ	10 11
	RAM_DQM_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
GROUP 3	MEM_DATA<31..24>	L:S:1233:1485	7	500	(200)			167 MHZ	9 10
	MEM_DQM<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	MEM_DQS<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167.0 MHz:::	9 10
	RAM_DATA_A<31..24>	L:S:1700:2165	7	500	(200)			167 MHZ	10 11
	RAM_DQM_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DATA_B<25..24>	L:S:1907:2356	7	500	(200)			167 MHZ	10 11
	RAM_DATA_B<26>	L:S:1907 MIL:2356 MIL	7		(200)			167.0 MHz:::	10 11
	RAM_DATA_B<31..27>	L:S:1907:2356	7	500	(200)			167 MHZ	10 11
	RAM_DQM_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
GROUP 4	MEM_DATA<39..32>	L:S:1915:2000	7	500	(200)			167 MHZ	9 10
	MEM_DQM<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	MEM_DQS<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167.0 MHz:::	9 10
	RAM_DATA_A<39..32>	L:S:1205:1387	7	500	(200)			167 MHZ	10 11
	RAM_DQM_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
DDR RAM	RAM_DQS_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DATA_B<39..32>	L:S:1404:1686	7	500	(200)			167 MHZ	10 11
	RAM_DQM_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
GROUP 5	MEM_DATA<47..40>	L:S:1719:1893	7	500	(200)			167 MHZ	9 10
	MEM_DQM<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	MEM_DQS<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167.0 MHz:::	9 10
	RAM_DATA_A<47..40>	L:S:1607:1898	7	500	(200)			167 MHZ	10 11
	RAM_DQM_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DATA_B<47..40>	L:S:1716:2102	7	500	(200)			167 MHZ	10 11
	RAM_DQM_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
GROUP 6	MEM_DATA<55..48>	L:S:2101:2170	7	500	(200)			167 MHZ	9 10
	MEM_DQM<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	MEM_DQS<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167.0 MHz:::	9 10
	RAM_DATA_A<55..48>	L:S:1204:1357	7	500	(200)			167 MHZ	10 11
	RAM_DQM_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DATA_B<55..48>	L:S:1400:1546	7	500	(200)			167 MHZ	10 11
	RAM_DQM_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
GROUP 7	MEM_DATA<63..56>	L:S:1903:2000	7	500	(200)			167 MHZ	9 10
	MEM_DQM<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	MEM_DQS<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167.0 MHz:::	9 10
	RAM_DATA_A<63..56>	L:S:1611:1696	7	500	(200)			167 MHZ	10 11
	RAM_DQM_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DATA_B<63..56>	L:S:1809:1887	7	500	(200)			167 MHZ	10 11
	RAM_DQM_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
ADDR	MEM_ADDR<12..0>	L:S::500	4					83 MHZ	9
	RAM_ADDR<12..0>	L:S:2000:3000	10		(200)				9 11
	MEM_BA<1..0>	L:S::500	4						9
	RAM_BA<1..0>	L:S:2000:3300	8		(200)				9 11
CONTROL	MEM_CS_L<3..0>	L:S::500	4						9
	RAM_CS_L<3..0>	L:S:2500:3200	7		(200)				9 11
	MEM_CKE<3..0>	L:S::500	4						9
	RAM_CKE<3..0>	L:S:2500:3200	7		(200)				9 11
	MEM_RAS_L	L:S::500 MIL	4						9
	RAM_RAS_L	L:S:2000 MIL:4100 MIL	7		(200)				9 11
	MEM_CAS_L	L:S::500 MIL	4						9
	RAM_CAS_L	L:S:2000 MIL:4100 MIL	7		(200)				9 11
	MEM_WE_L	L:S::500 MIL	4						9
	RAM_WE_L	L:S:2000 MIL:3100 MIL	8		(200)				9 11
	MEM_MUXSEL_MSB	L:S:1700 MIL:3000 MIL	8						9 10
	MEM_MUXSEL_LSB	L:S:1700 MIL:3000 MIL	7						9 10

PRIORITY: 2
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE
EXPOSED ROUTES
MINIMIZE VIAS

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	PROPAGATION_DELAY	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF	L:S::150 MIL					10 MIL SPACING	167.0 MHz:::	8
	SYSCLK_CPU	L:S:2650 MIL:2750 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	5 8
	INT_CPUFB_OUT	L:S::150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::	8
	INT_CPUFB_OUT_SHORT	L:S:700 MIL:850 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::	8
	INT_CPUFB_OUT_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::	8
	INT_CPUFB_IN_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::	8
	INT_CPUFB_LONG	L:S:1050 MIL:1150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::	8
	INT_CPUFB_IN	L:S:700 MIL:800 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	8
	SYSCLK_DDRCLK_A0_UF	L:S:300 MIL:300 MIL	SYSCLK_DDRCLK_A0_UF	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_A0_L_UF	L:S:300 MIL:300 MIL	SYSCLK_DDRCLK_A0_UF	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_A1_UF	L:S:300 MIL:300 MIL	SYSCLK_DDRCLK_A1_UF	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_A1_L_UF	L:S:300 MIL:300 MIL	SYSCLK_DDRCLK_A1_UF	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_B0_UF	L:S:300 MIL:300 MIL	SYSCLK_DDRCLK_B0_UF	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_B0_L_UF	L:S:300 MIL:300 MIL	SYSCLK_DDRCLK_B0_UF	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_B1_UF	L:S:300 MIL:300 MIL	SYSCLK_DDRCLK_B1_UF	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_B1_L_UF	L:S:300 MIL:300 MIL	SYSCLK_DDRCLK_B1_UF	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_A0_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_A1_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_B0_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_B1_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	INT_REF_CLK_OUT_UF	L:S::400 MIL				(200)	10 MIL SPACING	49.92 MHz:::	14
	INT_REF_CLK_OUT	L:S:1000 MIL:1150 MIL		5	250.0000	(200)	10 MIL SPACING	49.92 MHz:::	14
	INT_REF_CLK_IN	L:S:1900 MIL:2000 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	14
	CLK66M_GPU_AGP_UF	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz:::	12
	CLK66M_GPU_AGP	L:S:1800 MIL:1900 MIL		6	400.0000	(200)	10 MIL SPACING	66.00 MHz:::	12 19
	INT_AGP_FB_OUT	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz:::	12
	INT_AGP_FB_IN	L:S:1450 MIL:1550 MIL		6	500.0000	(200)	10 MIL SPACING	66.00 MHz:::	12
	CLK33M_CBUS_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz:::	12
	CLK33M_CBUS	L:S:5000 MIL:6000 MIL		9	500.0000	(200)	10 MIL SPACING	33.00 MHz:::	12 18
	CLK33M_AIRPORT_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz:::	12
	CLK33M_AIRPORT	L:S:9500 MIL:10500 MIL		6	500.0000	(200)	10 MIL SPACING	33.00 MHz:::	12 24 39
	CLK33M_NEC_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz:::	12
	CLK33M_NEC	L:S:4000 MIL:6000 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz:::	12 17
	INT_PCI_FB_OUT	L:S::300 MIL				(200)	10 MIL SPACING	33.00 MHz:::	12
	INT_PCI_FB_IN	L:S:6500 MIL:7500 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz:::	12
M10 & OSC	ATI_CLK27M_OSC	L:S::400 MIL		5		(200)	10 MIL SPACING		19
	ATI_CLK27M_OSC_SS	L:S::400 MIL		5		(200)	10 MIL SPACING		19
	ATI_CLK27M_IN	L:S::200 MIL		5		(200)	10 MIL SPACING		19 20
	ATI_SSCLK_UF	L:S::200 MIL		5		(200)	10 MIL SPACING		19
	ATI_SSCLK_IN	L:S::1800 MIL		5	500.0000	(200)	10 MIL SPACING		19 20
CRYSTALS	CLK18M_INT_XIN	L:S:1400 MIL:1500 MIL					10 MIL SPACING		14
	CLK18M_INT_XOUT	L:S:1250 MIL:1350 MIL					10 MIL SPACING		14
	CLK18M_XTAL_IN	L:S::300 MIL					10 MIL SPACING		14
	CLK18M_INT_EXT	L:S::400 MIL					10 MIL SPACING		14
SOUND	INT_I2S0_SND_MCLK			6	500.0000	(200)	10 MIL SPACING		14 25 39
ETHERNET	CLKENET_PHY_RX	L:S::300 MIL				(200)		125.0 MHz:::	26
	CLKENET_LINK_RX	L:S:8000 MIL:9000 MIL		6	800.0000	(200)	10 MIL SPACING	125.0 MHz:::	13 26
	CLKENET_PHY_GBE_REF	L:S::300 MIL				(200)		125.0 MHz:::	26
	CLKENET_LINK_GBE_REF	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	125.0 MHz:::	13 26
	CLKENET_PHY_TX	L:S::300 MIL				(200)		25.00 MHz:::	26
	CLKENET_LINK_TX	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	25.00 MHz:::	13 26
	CLKENET_LINK_GTX	L:S::300 MIL				(200)		125.0 MHz:::	13
	CLKENET_PHY_GTX	L:S:8000 MIL:9000 MIL		6	600.0000	(200)	10 MIL SPACING	125.0 MHz:::	13 26
FIREWIRE	CLKFW_PHY_PCLK	L:S::300 MIL				(200)		49.15 MHz:::	27
	CLKFW_LINK_PCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz:::	13 27
	CLKFW_PHY_LCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz:::	13 27
	CLKFW_LINK_LCLK	L:S::300 MIL				(200)		49.15 MHz:::	13
	FW_XI	L:S::500 MIL				(200)	10 MIL SPACING	98.03 MHz:::	27
	FW_OSC	L:S::300 MIL				(200)	10 MIL SPACING	98.03 MHz:::	27

PRIORITY: 1
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE EXPOSURE ON LONG NETS

SIGNAL CONSTRAINTS - PAGE 1

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D	051-6537	B
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EXT. TMDS/DVO signal constraints

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
MAXBUS	CPU_AACK_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ
	CPU_ARTRY_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_BG_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_BR_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_CI_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ
	CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ
	CPU_DBG_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_DTI<0..2>	L:S:1500:2950	7		(250)			
	CPU_DRDY_L	L:S:1500 MIL:3200 MIL	7		(250)			
	CPU_GBL_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_HIT_L	L:S:1500 MIL:2800 MIL	7		(250)			
	CPU_QACK_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_QREQ_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TA_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TBST_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TEA_L	L:S:1500 MIL:3000 MIL	7		(250)			
	CPU_TS_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)			
	CPU_TT<0..4>	L:S:1500:3400	7		(250)			
	CPU_WT_L	L:S:1500 MIL:3100 MIL	7		(250)			

STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALES

1233	GPU_TMDS_CLKN	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	5	19 20
1233	GPU_TMDS_CLKP	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	5	19 20
1232	GPU_TMDS_DN<0>	GPU_TMDS_D0	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	8	19 20
1234	GPU_TMDS_DP<0>	GPU_TMDS_D0	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	8	19 20
1235	GPU_TMDS_DN<1>	GPU_TMDS_D1	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	8	19 20
1236	GPU_TMDS_DP<1>	GPU_TMDS_D1	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	8	19 20
1238	GPU_TMDS_DN<2>	GPU_TMDS_D2	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	8	19 20
1237	GPU_TMDS_DP<2>	GPU_TMDS_D2	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	8	19 20

1240	SI_TMDS_CLKN	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING 100 OHM SPACING	5	19
1239	SI_TMDS_CLKP	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING 100 OHM SPACING	5	19
1242	SI_TMDS_DN<0>	SI_TMDS_D0	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING 100 OHM SPACING	8	19
1241	SI_TMDS_DP<0>	SI_TMDS_D0	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING 100 OHM SPACING	8	19
1243	SI_TMDS_DN<1>	SI_TMDS_D1	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING 100 OHM SPACING	8	19
1245	SI_TMDS_DP<1>	SI_TMDS_D1	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING 100 OHM SPACING	8	19
1244	SI_TMDS_DN<2>	SI_TMDS_D2	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING 100 OHM SPACING	8	19
1246	SI_TMDS_DP<2>	SI_TMDS_D2	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING 100 OHM SPACING	8	19

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

1263	ATI_DVOD<11..0>	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610		19 20
1260	ATI_DVOD_DE	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		19 20
1264	ATI_DVO_HSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		19 20
1267	ATI_DVO_VSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		19 20
1266	ATI_DVO_CLKP	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000	165.0 MHz:::	19 20

1258	GPU_DVOD<11..0>	GPUDVOD:G:L:S:0 MIL:50 MIL	6	700		19
1259	GPU_DVOD_DE	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		19
1260	GPU_DVO_HSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		19
1261	GPU_DVO_VSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		19
1262	GPU_DVO_CLKP	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000	165.0 MHz:::	19

1268	TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	4	22 39
1269	TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	4	22 39
1271	TMDS_CONN_DN<0>	CONN_TMDS_D0	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	4	22
1270	TMDS_CONN_DP<0>	CONN_TMDS_D0	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	4	22
1272	TMDS_CONN_DN<1>	CONN_TMDS_D1	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	4	22
1273	TMDS_CONN_DP<1>	CONN_TMDS_D1	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	4	22
1274	TMDS_CONN_DN<2>	CONN_TMDS_D2	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	4	22
1275	TMDS_CONN_DP<2>	CONN_TMDS_D2	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	4	22

SIGNAL CONSTRAINTS - PAGE 1

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Digital Signals (cont'd)

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
AGP	AGP_AD<15..0>	L:S:1050:1450	7					66 MHZ 12 19
AGP BYTES 0-1	AGP_CBE<1..0>	L:S:1050:1450	7					66 MHZ 12 19
	AGP_AD_STB<0>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ 12 19
	AGP_AD_STB_L<0>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ 12 19
AGP BYTES 2-3	AGP_AD<31..16>	L:S:1050:1450	7					66 MHZ 12 19
	AGP_CBE<3..2>	L:S:1050:1450	7					66 MHZ 12 19
	AGP_AD_STB<1>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ 12 19
	AGP_AD_STB_L<1>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ 12 19
AGP SIDEBAND	AGP_SBA<7..0>	L:S:1050:1450	7					66 MHZ 12 19
	AGP_SB_STB	L:S:1050 MIL:1450 MIL			(350)	8 MIL SPACING		66.00 MHZ 12 19
	AGP_SB_STB_L	L:S:1050 MIL:1450 MIL			(350)	8 MIL SPACING		66.00 MHZ 12 19
AGP CONTROL	AGP_FRAME_L	L:S:1250 MIL:1950 MIL						66.00 MHZ 12 19
	AGP_IRDY_L	L:S:1250 MIL:1950 MIL						66.00 MHZ 12 19
	AGP_TRDY_L	L:S:1250 MIL:1950 MIL						66.00 MHZ 12 19
	AGP_DEVSEL_L	L:S:1250 MIL:1950 MIL						66.00 MHZ 12 19
	AGP_STOP_L	L:S:1250 MIL:1950 MIL						66.00 MHZ 12 19
	AGP_PAR	L:S:1250 MIL:1950 MIL						66.00 MHZ 12 19
	AGP_REQ_L	L:S:1250 MIL:1950 MIL						66.00 MHZ 12 19
	AGP_GNT_L	L:S:1250 MIL:1950 MIL						66.00 MHZ 12 19
	AGP_RBF_L	L:S:1250 MIL:1950 MIL						66.00 MHZ 12 19
PCI	PCI_AD<31..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ 9 12 17 18 24 39
	PCI_CBE<3..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ 12 17 18 24
	PCI_FRAME_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ 12 17 18 24 39
	PCI_IRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ 12 17 18 24 39
	PCI_TRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ 12 17 18 24 39
	PCI_DEVSEL_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ 12 17 18 24 39
	PCI_STOP_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ 12 17 18 24 39
	PCI_PAR	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ 12 17 18 24 39
ULTRA ATA-100	UIDE_DATA<15..8>	L:S::710			(200)			100 MHZ 13 24
	UIDE_DATA<7>	U51.V1:RP19.3::600 MIL			(200)			100.0 MHZ 13 24
	UIDE_DATA<6..0>	L:S::600			(200)			100 MHZ 13 24
	UIDE_ADDR<2..0>	L:S::650			(200)			100 MHZ 13 24
	UIDE_RST_L	L:S::400 MIL			(200)			100.0 MHZ 13 24
	UIDE_DIOW_L	L:S::400 MIL			(200)			100.0 MHZ 13 24
	UIDE_DIOR_L	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ 13 24
	UIDE_DMACK_L	L:S::400 MIL			(200)			100.0 MHZ 13 24
	UIDE_CS0_L	L:S::500 MIL			(200)			100.0 MHZ 13 24
	UIDE_CS1_L	L:S::500 MIL			(200)			100.0 MHZ 13 24
	UIDE_DMARQ	L:S::400 MIL			(200)			100.0 MHZ 13
	UIDE_IOCHRDY	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ 13 24
	UIDE_INTRQ	L:S::400 MIL			(200)			100.0 MHZ 13
	HD_DATA<15..0>	L:S:5000:6500	7		(200)			100 MHZ 24
	HD_ADDR<2..0>	L:S:5000:6500	7		(200)			100 MHZ 24
	HD_RESET_L	L:S:4000 MIL:6000 MIL			(200)			100.0 MHZ 24
	HD_DIOW_L	L:S:3000 MIL:5200 MIL			(200)			100.0 MHZ 24
	HD_DIOR_L	L:S:6100 MIL:6150 MIL		10 MIL SPACING	(200)			100.0 MHZ 24
	HD_DMACK_L	L:S:4500 MIL:6000 MIL			(200)			100.0 MHZ 24
	HD_CS0_L	L:S:3000 MIL:6000 MIL			(200)			100.0 MHZ 24
	HD_CS1_L	L:S:3000 MIL:6000 MIL			(200)			100.0 MHZ 24
	HD_DMARQ	L:S:4500 MIL:6000 MIL			(200)			100.0 MHZ 13 24
	HD_IOCHRDY	L:S:6200 MIL:6300 MIL		10 MIL SPACING	(200)			100.0 MHZ 24
	HD_INTRQ	L:S:3000 MIL:5000 MIL						100.0 MHZ 13 24
EIDE INTREPID	EIDE_DATA<15..0>	L:S::850						33 MHZ 13 24
	EIDE_ADDR<2..0>	L:S::850						33 MHZ 13 24
	EIDE_CS0_L	L:S::850 MIL						33.00 MHZ 13 24
	EIDE_CS1_L	L:S::850 MIL						33.00 MHZ 13 24
	EIDE_RD_L	L:S::500 MIL						33.00 MHZ 13 24
	EIDE_WR_L	L:S::500 MIL						33.00 MHZ 13 24
	EIDE_IOCHRDY	L:S::500 MIL						33.00 MHZ 13 24
	EIDE_INT	L:S::500 MIL						33.00 MHZ 13 24
	EIDE_RST_L	L:S::500 MIL						33.00 MHZ 13 24
	EIDE_DMACK_L	L:S::500 MIL						33.00 MHZ 13 24
	EIDE_DMARQ	L:S::500 MIL						33.00 MHZ 13 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>	L:S:4000:6000						33 MHZ 24 39
	EIDE_OPTICAL_ADDR<2..0>	L:S:4000:6000						33 MHZ 24 39
	EIDE_OPTICAL_CS0_L	L:S:4500 MIL:6500 MIL						33.00 MHZ 24 39
	EIDE_OPTICAL_CS1_L	L:S:4500 MIL:6500 MIL						33.00 MHZ 24 39
	EIDE_OPTICAL_READ_L	L:S:4500 MIL:6500 MIL						33.00 MHZ 24 39
	EIDE_OPTICAL_WR_L	L:S:4500 MIL:6500 MIL						33.00 MHZ 24 39
	EIDE_OPTICAL_IOCHRDY	L:S:4500 MIL:6500 MIL						33.00 MHZ 24 39
	EIDE_OPTICAL_INT	L:S:5000 MIL:7000 MIL						33.00 MHZ 24 39
	EIDE_OPTICAL_RST_L	L:S:4500 MIL:6500 MIL						33.00 MHZ 24 39
	EIDE_OPTICAL_DMACK_L	L:S:4500 MIL:6500 MIL						33.00 MHZ 24 39
	EIDE_OPTICAL_DMA_RQ	L:S:4500 MIL:6500 MIL						33.00 MHZ 24 39
ETHERNET MII	ENET_LINK_RXD<7..0>	L:S:8000:9000	7	(400)		(400)		13 26
	ENET_RX_DV	L:S:8000 MIL:9000 MIL						13 26
	ENET_RX_ER	L:S:8000 MIL:9000 MIL						13 26
	ENET_PHY_TXD<7..0>	L:S:8000:9000	7	(400)		(400)		13 26
	ENET_LINK_TXD<7..0>	L:S::600						13
	ENET_PHY_TX_ER	L:S:8000 MIL:9000 MIL						13 26
	ENET_LINK_TX_ER	L:S::400 MIL						13
	ENET_PHY_TX_EN	L:S:8000 MIL:9000 MIL						13 26
	ENET_LINK_TX_EN	L:S::400 MIL						13
	ENET_MDIO	L:S:8000 MIL:9000 MIL						13 26
	ENET_MDC	L:S:8000 MIL:9000 MIL						13 26
	ENET_COL	L:S:8000 MIL:9000 MIL						13 26
	ENET_CRS	L:S:8000 MIL:9000 MIL						13 26
FIREWIRE MII	FW_LINK_DATA<7..0>	L:S:2700:3500	7	(400)		(400)		13 27
	FW_PHY_DATA<7..0>	L:S:4700:5500	7	(400)		(400)		27
	FW_LINK_CNTL<1..0>	L:S:9000:10000						13 27
	FW_PHY_CNTL<1..0>	L:S::300						27
	FW_LINK_LREQ	L:S::300 MIL						13
	FW_PHY_LREQ	L:S:8500 MIL:9500 MIL						13 27
	FW_PINT	L:S:8500 MIL:9500 MIL						13 27

NEED TO MATCH DELAY TO 250

TOTAL UIDE+HD SKEW <500MIL

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

PRIORITY: 7
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 6
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 8
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	RELATIVE_PROPAGATION_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS
FIREWIRE Zo = 110	FW_TPI0N	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	27 28 39
	FW_TPI0P	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	27 28 39
	FW_TPO0N	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	27 28 39
	FW_TPO0P	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	27 28 39
	FW_TPBI0N	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	28
	FW_TPBI0P	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	28
	FW_TPAO0N	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	28
	FW_TPAO0P	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	28
	FW_TPA1N	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	27 28
	FW_TPA1P	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	27 28
	FW_TPB1N	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	27 28
	FW_TPB1P	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	27 28
	FW_TPI1N	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	28 39
	FW_TPI1P	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	28 39
	FW_TPO1N	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	28 39
	FW_TPO1P	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	28 39
ETHERNET Zo = 100	MDI_P<0>	ENET_MDI0	ENET_MDI0:G:U43.29:J23.1:0 MIL:100 MIL		ENET 10 MIL SPACING	26 39
	MDI_M<0>	ENET_MDI0	ENET_MDI0:G:U43.31:J23.2:0 MIL:100 MIL		ENET 10 MIL SPACING	26 39
	MDI_P<1>	ENET_MDI1	ENET_MDI1:G:U43.33:J23.3:0 MIL:100 MIL		ENET 10 MIL SPACING	26 39
	MDI_M<1>	ENET_MDI1	ENET_MDI1:G:U43.34:J23.4:0 MIL:100 MIL		ENET 10 MIL SPACING	26 39
	MDI_P<2>	ENET_MDI2	ENET_MDI2:G:U43.39:J23.7:0 MIL:100 MIL		ENET 10 MIL SPACING	26 39
	MDI_M<2>	ENET_MDI2	ENET_MDI2:G:U43.41:J23.8:0 MIL:100 MIL		ENET 10 MIL SPACING	26 39
	MDI_P<3>	ENET_MDI3	ENET_MDI3:G:U43.42:J23.9:0 MIL:100 MIL		ENET 10 MIL SPACING	26 39
	MDI_M<3>	ENET_MDI3	ENET_MDI3:G:U43.43:J23.10:0 MIL:100 MIL		ENET 10 MIL SPACING	26 39
LVDS Zo = 100 LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 4	20 22 39
	CLKLVDS_LP	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 4	20 22 39
	LVDS_L0N	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	20 22 39
	LVDS_L0P	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	20 22 39
	LVDS_L1N	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	20 22 39
	LVDS_L1P	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	20 22 39
	LVDS_L2N	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	20 22 39
	LVDS_L2P	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	20 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 4	20 22
	CLKLVDS_UP	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 4	20 22
	LVDS_U0N	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	20 22
	LVDS_U0P	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	20 22
	LVDS_U1N	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	20 22
	LVDS_U1P	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	20 22
	LVDS_U2N	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	20 22
	LVDS_U2P	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	20 22
TMDS Zo = 100	TMDS_CLKN	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 5	19 22
	TMDS_CLKP	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 5	19 22
	TMDS_DN<0>	TMDS_D0	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 8	19 22 39
	TMDS_DP<0>	TMDS_D0	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 8	19 22 39
	TMDS_DN<1>	TMDS_D1	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 8	19 22 39
	TMDS_DP<1>	TMDS_D1	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 8	19 22 39
	TMDS_DN<2>	TMDS_D2	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 8	19 22 39
	TMDS_DP<2>	TMDS_D2	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 8	19 22 39
	1240 ATI_TMDS_CLKN	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING 5	20
	1240 ATI_TMDS_CLKP	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING 5	20
	1240 ATI_TMDS_DN<0>	ATI_TMDS_D0	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING 8	20
	1240 ATI_TMDS_DP<0>	ATI_TMDS_D0	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING 8	20
	1240 ATI_TMDS_DN<1>	ATI_TMDS_D1	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING 8	20
	1240 ATI_TMDS_DP<1>	ATI_TMDS_D1	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING 8	20
	1240 ATI_TMDS_DN<2>	ATI_TMDS_D2	ATITMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 8	20
	1240 ATI_TMDS_DP<2>	ATI_TMDS_D2	ATITMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 8	20
USB 1.1 Zo = 90	USB_DEM	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		10 MIL SPACING	14
	USB_DEP	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		10 MIL SPACING	14
	USB_DFM	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		10 MIL SPACING	14
	USB_DFP	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		10 MIL SPACING	14
	BT_USB_DM	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING	14 25 39
	BT_USB_DP	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING	14 25 39
USB 2.0 Zo = 90	MODEM_USB_DM	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING	14 25 39
	MODEM_USB_DP	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING	14 25 39
	NEC_USB_DAM	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	17 25 39
	NEC_USB_DAP	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	17 25 39
	NEC_USB_DBM	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	17 25 39
	NEC_USB_DBP	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	17 25 39
POWER SUPPLIES	1772_CSSN	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL			30
	1772_CSSP	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL			30
	1772_CSIN	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL			30
	1772_CSIP	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL			30
	3V_SNSM	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL			32
	3V_SNSP	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL			32
	5V_SNSM	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL			32
	5V_SNSP	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL			32
THERMOSTAT	THERM1_DM		THERM1:G:L:S:0 MIL:100 MIL			25
	THERM1_DP		THERM1:G:L:S:0 MIL:100 MIL			25
	THERM2_DM		THERM2:G:L:S:0 MIL:100 MIL			25
	THERM2_DP		THERM2:G:L:S:0 MIL:100 MIL			25
	THERM1_M_DM	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL			25
	THERM1_M_DP	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL			25
	THERM2_M_DM	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL			25
	THERM2_M_DP	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL			25
	THERM1_A_DM	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL			25
	THERM1_A_DP	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL			25
	THERM2_A_DM	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL			25
	THERM2_A_DP	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL			25

PRIORITY: 3
PRIMARY LAYERS: 4,7 FOR CONTROLLED IMPEDANCE DIFF PAIRS
SECONDARY LAYERS: 2,9 FOR UNCONTROLLED IMPEDANCE DIFF PAIRS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3MIL (TRACE WIDTH)
S = 11MIL (TRACE SEPERATION)
H = 16.8MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 106.2 OHMS
Zo(single) = 55.4 OHMS

Clear adjacent power plane!
Zo will be lower due to asymmetric stackup.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.1MIL (TRACE WIDTH)
S = 4.9MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 94 OHMS
Zo(single) = 50 OHMS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.6MIL (TRACE WIDTH)
S = 7MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 89.8 OHMS
Zo(single) = 46.6 OHMS

LAYERS 2 OR 9

SIGNAL CONSTRAINTS - PAGE 2

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SIZE	DRAWING NUMBER	REV.
D	051-6537	B
SCALE NONE	SHT 37 OF 44	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 39
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 31 39
	1347 +ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		30
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	30
PMU	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		30
	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		29 31
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		31 32
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		31
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		31
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 29
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 32
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22 39
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
AUDIO	1387 +5V_MAIN_AUD	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	1388 +3V_MAIN_AUD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	1389 AUD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50		25
FAN	1400 +FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39

I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	IN	
	CHGND1				
INVERTER	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	
	CHGND2				
TRACKPAD	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	
	CHGND3				
LVDS	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	
	CHGND4				

ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 33 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 7 8 15 16 33
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	1333 +2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 19
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
AIRPORT	+3V_AIRPORT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19 20 39
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 19 20 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 21
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 20 21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	1840 +GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1847 +2_5V_SLEEP_NECK1	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		20
	1848 +3V_SLEEP_NECK	VOLTAGE=3V	MIN_LINE_WIDTH=10		34
	1849 +1_5V_AGP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	1850 +1_8V_PVDD_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		20
	1851 GPU_VCORE_NECK	VOLTAGE=1.2V	MIN_LINE_WIDTH=10		20
	1852 +GPU_VDD15_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	1853 +2_5V_SLEEP_NECK2	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		34
	1854 +1_8V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		34
	1855 +1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		34
	1860 +1_8V_ATI_TPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	1861 +1_8V_GPU_TP_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
ETHERNET 88E1111 NEC USB2.0	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	1816 +3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	1817 NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	17
FW	1372 LM2594_IN	VOLTAGE=33V	MIN_LINE_WIDTH=40	MIN_NECK_WIDTH=12	27
	1313 +FW_PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	1345 +FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	27 28
	1316 +FW_PWR1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 28
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	1315 FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	1350 FW_VDD_ON	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1625_VSW	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	30 31
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
MAX1715 2.5V SWITCHER	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
1.65V SWITCHER	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		34
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
CONTROL	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	1_5V_ILIM		MIN_LINE_WIDTH=8		34
	2_5V_ILIM		MIN_LINE_WIDTH=8		34
	MAX1715_TON		MIN_LINE_WIDTH=8		34
	MAX1715_SKIP		MIN_LINE_WIDTH=8		34
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		34
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	33
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_ILIM		MIN_LINE_WIDTH=8		33
	VCORE_REF		MIN_LINE_WIDTH=8		33
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		33
	VCORE_CC		MIN_LINE_WIDTH=8		33
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33 39
	VCORE_TIME		MIN_LINE_WIDTH=8		33
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 33
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		33
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	1319 VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	20
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	1778_ION		MIN_LINE_WIDTH=8		20
	1778_ITH		MIN_LINE_WIDTH=8		20
	1778_ITH_RC		MIN_LINE_WIDTH=8		20
	1778_VFB		MIN_LINE_WIDTH=8		20 39
	1778_FCB		MIN_LINE_WIDTH=8		20
	1778_VRNG		MIN_LINE_WIDTH=8		20
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
LTC1962 INT PLLS	1_8V_VFB		MIN_LINE_WIDTH=8		34
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		34
	LTC3411_ITH		MIN_LINE_WIDTH=8		34
	LTC3411_SYNC		MIN_LINE_WIDTH=8		34
	LTC3411_SHDN		MIN_LINE_WIDTH=8		34
	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14

SIGNAL CONSTRAINTS - PAGE 3

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SIZE	DRAWING NUMBER	REV.
D	051-6537	B
SCALE NONE	SHT 38 OF 44	

FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.

FUNC_TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC_QTY IS FOR REFERENCE AND LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR. FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
SCAN/TEST	I2 JTAG_ASIC_TMS	TRUE			13 26
	I3 JTAG_ASIC_TDI	TRUE			13
	I1 JTAG_ASIC_TDO_TP	TRUE			26
	I4 JTAG_ASIC_TCK	TRUE			13 26
	I6 JTAG_ASIC_TRST_L	TRUE			13 26
	I5 CPU_CHKSTP_OUT_L	TRUE			5
	I7 CPU_SRESET_L	TRUE			5
	I9 CPU_HRESET_L	TRUE			5 6 7
	I8 JTAG_CPU_TMS	TRUE			5 6
	I10 JTAG_CPU_TDI	TRUE			5 6
	I12 JTAG_CPU_TDO_TP	TRUE			5
	I11 JTAG_CPU_TCK	TRUE			5 6
	I13 JTAG_CPU_TRST_L	TRUE			5 6
	I18 INT_JTAG_TEI	TRUE			13
	I20 INT_TST_MONIN_PD	TRUE			13
	I19 INT_TST_MONOUT_TP	TRUE			13
	I21 INT_TST_PLLEN_PD	TRUE			13
INT I2C	I15 INT_I2C_CLK0	TRUE			6 11 13 23
	I14 INT_I2C_DATA0	TRUE			6 11 13 23
	I16 INT_I2C_CLK1	TRUE			13 14 25
	I17 INT_I2C_DATA1	TRUE			13 14 25
PWR/GND	I216 +PBUS	TRUE			38
	I216 +24V_PBUS	TRUE			38
	I25 GPU_VCORE	TRUE			19 20 38
	I24 1778_VFB	TRUE			20 38
	I27 CPU_VCORE_SLEEP	TRUE			5 33 38
	I26 VCORE_FB	TRUE			33 38
	I213 +1_8V_MAIN	TRUE			38
	I218 +2_5V_MAIN	TRUE			38
	I219 +5V_MAIN	TRUE	2		38 39
	I220 +5V_SLEEP	TRUE	2		38 39
	I221 +3V_MAIN	TRUE	4	1000	23 38
		TRUE			IN
	I222 +3V_PMU	TRUE			38
CARDBUS	I36 CBUS_DET_1_L	TRUE		2000	18
	I35 CBUS_DET_2_L	TRUE		2000	18
DVI	I37 TMDS_DN<0..2>	TRUE		1000	19 22 37
	I38 TMDS_DP<0..2>	TRUE		1000	19 22 37
	I40 TMDS_CONN_CLKN	TRUE		1000	22 36
	I39 TMDS_CONN_CLKP	TRUE		1000	22 36
	I42 VGA_R	TRUE		1000	22
	I41 VGA_G	TRUE		1000	22
	I44 VGA_B	TRUE		1000	22
	I43 VGA_HSYNC	TRUE		1000	22
	I46 VGA_VSYNC	TRUE		1000	22
	I45 DVI_DDC_CLK_UF	TRUE		1000	22
	I47 DVI_DDC_DATA_UF	TRUE		1000	22
	I48 DVI_HPD_UF	TRUE		1000	22
	I49 +5V_DDC_SLEEP	TRUE		2000	22 38
		TRUE	2	2000	IN
		TRUE	6	1000	IN
CHGND1 LVDS	I52 LVDS_L0N	TRUE		1000	20 22 37
	I51 LVDS_L0P	TRUE		1000	20 22 37
	I53 LVDS_L1N	TRUE		1000	20 22 37
	I55 LVDS_L1P	TRUE		1000	20 22 37
	I54 LVDS_L2N	TRUE		1000	20 22 37
	I57 LVDS_L2P	TRUE		1000	20 22 37
	I56 CLKLVDS_LN	TRUE		1000	20 22 37
	I58 CLKLVDS_LP	TRUE		1000	20 22 37
	I59 LVDS_DDC_CLK	TRUE		1000	20 22
	I60 LVDS_DDC_DATA	TRUE		1000	20 22
	I62 +3V_LCD	TRUE	2	2000	22 38
	I223 +3V_SLEEP	TRUE		2000	38 39
		TRUE	2	2000	IN
		TRUE	6	1000	IN
CHGND4 INVERTER	I67 +14V_INV	TRUE		2000	22 38
	I66 +5V_INV_SW	TRUE		2000	22 38
	I68 BRIGHT_PWM	TRUE		2000	22
	I249 INV_GND	TRUE		2000	22
		TRUE		1000	IN
S-VIDEO	I70 TV_C	TRUE		2000	22
	I72 TV_Y	TRUE		2000	22
	I71 TV_COMP	TRUE		2000	22
	I73 TV_GND1	TRUE		2000	22 38
	I74 TV_GND2	TRUE		2000	22 38
LIO	I76 INT_I2S0_SND_TO_DAC	TRUE		1000	14 25
	I75 INT_I2S0_SND_LRCLK	TRUE		1000	14 25
	I78 INT_I2S0_SND_MCLK	TRUE		1000	14 25 35
	I83 INT_I2S0_SND_SCLK	TRUE		1000	14 25
	I82 INT_I2S0_SND_FROM_ADC	TRUE		1000	14 25
	I77 SND_HP_MUTE_L	TRUE		1000	14 25
	I79 SND_AMP_MUTE	TRUE		1000	25
	I84 SND_HW_RESET_L	TRUE		1000	14 25
	I85 SND_HP_SENSE_L	TRUE		1000	14 25
	I86 SND_LIN_SENSE_L	TRUE		1000	14 25
	I81 INT_I2C_CLK2	TRUE		1000	14 25
	I80 INT_I2C_DATA2	TRUE		1000	14 25
	I87 ADAPTER_DET	TRUE		1000	25 29
	I88 CHARGE_LED_L	TRUE		1000	25 29
	I89 NEC_LUSB_OCI_UF	TRUE		1000	17 25
	I90 NEC_LUSB_PPON	TRUE		1000	17 25
	I223 +5V_MAIN	TRUE	2	2000	38 39
	I225 +5V_SLEEP	TRUE	2	3000	38 39
	I226 +3V_SLEEP	TRUE		2000	38 39

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
USB	I94 NEC_USB_DAM	TRUE			17 25 37
	I96 NEC_USB_DAP	TRUE			17 25 37
	I95 NEC_USB_DBM	TRUE			17 25 37
	I97 NEC_USB_DBP	TRUE			17 25 37
	I98 BT_USB_DM	TRUE			14 25 37
	I99 BT_USB_DP	TRUE			14 25 37
	I100 MODEM_USB_DM	TRUE			14 25 37
	I101 MODEM_USB_DP	TRUE			14 25 37
RT. USB	I102 NEC_RUSB_PPON	TRUE			17 25
	I103 NEC_RUSB_OCI_UF	TRUE			17 25
WIRELESS	I105 PCI_AD<0..31>	TRUE		1000	9 12 17 18 24 37
	I106 PCI_FRAME_L	TRUE		1000	12 17 18 24 37
	I108 PCI_TRDY_L	TRUE		1000	12 17 18 24 37
	I107 PCI_IRDY_L	TRUE		1000	12 17 18 24 37
	I109 PCI_DEVSEL_L	TRUE		1000	12 17 18 24 37
	I110 PCI_STOP_L	TRUE		1000	12 17 18 24 37
	I111 PCI_PAR	TRUE		1000	12 17 18 24 37
	I113 AIRPORT_PCI_REQ_L	TRUE		1000	12 24
	I112 AIRPORT_PCI_GNT_L	TRUE		1000	12 24
	I114 AIRPORT_PCI_INT_L	TRUE		1000	14 24
	I115 MAIN_RESET_L	TRUE		1000	14 17 18 19 24 29
	I116 CLK33M_AIRPORT	TRUE		1000	12 24 35
	I119 PMU_PME_L	TRUE		1000	14 17 24 29
	I117 ROM_ONBOARD_CS_L	TRUE		1000	9 24
	I118 ROM_OE_L	TRUE		1000	9 12 24
	I121 ROM_CS_L	TRUE		1000	9 12 24
	I122 ROM_RW_L	TRUE		1000	9 12 24
	I229 RF_DISABLE_L	TRUE		1000	24
	I230 AIRPORT_CLKRUN_L	TRUE		1000	24
	I120 +3V_AIRPORT	TRUE	4	2000	38
		TRUE	6	1000	IN
OPTICAL	I124 EIDE_OPTICAL_DATA<0..15>	TRUE		2000	24 37
	I125 EIDE_OPTICAL_DMA_RQ	TRUE		2000	24 37
	I126 EIDE_OPTICAL_READ_L	TRUE		2000	24 37
	I128 EIDE_OPTICAL_DMAACK_L	TRUE		2000	24 37
	I127 EIDE_OPTICAL_ADDR<0..2>	TRUE		2000	24 37
	I129 EIDE_OPTICAL_CS0_L	TRUE		2000	24 37
	I130 EIDE_OPTICAL_CS1_L	TRUE		2000	24 37
	I131 EIDE_OPTICAL_RST_L	TRUE		2000	24 37
	I133 EIDE_OPTICAL_WR_L	TRUE		2000	24 37
	I132 EIDE_OPTICAL_IOCHRDY	TRUE		2000	24 37
	I134 EIDE_OPTICAL_INT	TRUE		2000	24 37
TRACKPAD	I135 +5V_TPAD_SLEEP	TRUE		3000	23 38
	I136 TPAD_F_TXD	TRUE		3000	23
	I138 TPAD_F_RXD	TRUE		3000	23
	I137 LID_CLOSED_L	TRUE		3000	23
	I139 +3V_HALL_EFFECT	TRUE		3000	23 38
	I139 SOFT_PWR_ON_L	TRUE		3000	22 23 29 33
MODEM/ SERIAL	I141 COMM_RESET_L	TRUE		4000	14 25
	I140 COMM_SHUTDOWN	TRUE		4000	14 25
	I142 COMM_RING_DET_L	TRUE		4000	14 25 29
	I144 COMM_TXD_L	TRUE		4000	14 25
	I143 COMM_TRXC	TRUE		4000	14 25
	I146 COMM_GPIO_L	TRUE		4000	14 25
	I145 COMM_DTR_L	TRUE		4000	14 25
	I147 COMM_RTS_L	TRUE		4000	14 25
	I149 COMM_RXD	TRUE		4000	14 25
KEYBOARD	I154 KBD_ID	TRUE		3000	23 29
	I155 KBD_INTL	TRUE		3000	23
	I156 KBD_JIS	TRUE		3000	23
	I152 KBD_CAPSLOCK_LED	TRUE		3000	23
	I153 KBD_NUMLOCK_LED	TRUE		3000	23
	I158 KBD_FUNCTION_L	TRUE		3000	23 29
	I150 KBD_COMMAND_L	TRUE		3000	23 29
	I157 KBD_OPTION_L	TRUE		3000	23 29
	I151 KBD_CONTROL_L	TRUE		3000	23 29
	I159 KBD_SHIFT_L	TRUE		3000	23 29
	I160 KBD_X<0..9>	TRUE		3000	23 29
	I161 KBD_Y<0..7>	TRUE		3000	23 29
BATTERY	I166 +BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	I167 BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	I165 BATT_CLK	TRUE		1000	30
	I164 BATT_DATA	TRUE		1000	30
	I168 PMU_BATT_DET_L	TRUE		1000	29 30
FANS	I169 +FAN_PWR	TRUE		3000	25 38
	I170 FAN1_TACH	TRUE		3000	25
	I172 FAN2_TACH	TRUE		3000	25
	I171 FAN1_GND	TRUE		3000	38
	I173 FAN2_GND	TRUE		3000	38
ETHERNET	I174 MDI_P<0..3>	TRUE		1000	26 37
	I175 MDI_M<0..3>	TRUE		1000	26 37
FIREWIRE	I177 FW_TPO0P	TRUE		1000	27 28 37
	I176 FW_TPO0N	TRUE		1000	27 28 37
	I179 FW_TPO0R	TRUE		1000	28
	I178 FW_TPI0P	TRUE		1000	27 28 37
	I180 FW_TPI0N	TRUE		1000	27 28 37
	I182 +FW_VP0	TRUE		1000	28 38
	I181 FW_VGND	TRUE		1000	39

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
FIREWIRE (CONT.)	I183 FW_TPO1P	TRUE		1000	28 37
	I185 FW_TPO1N	TRUE		1000	28 37
	I187 FW_TPI1P	TRUE		1000	28 37
	I186 FW_TPI1N	TRUE		1000	28 37
	I184 +FW_VP1	TRUE		1000	28 38
	I188 FW_VGND	TRUE		1000	39
DC PWR IN	I189 +ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000	30 31 38
LMU/ALS	I250 ST7_SLEEP_LED_H	TRUE			23
	I250 PMU_SLEEP_LED	TRUE			23
	I250 PMU_LID_CLOSED_L	TRUE			23 29
	I250 LMU_DETECT	TRUE			23
		TRUE	6	1000	IN
MISC.			(100 MIL PROBE PREFERRED)		
	I192 SLEEP_LED	TRUE			23
	I193 PMU_KB_RESET_L	TRUE			29
	I190 SLEEP	TRUE			23 25 29 32 34
	I191 PMU_CPU_HRESET_L	TRUE			6 29
	I197 BB_RESET_L	TRUE			6
	I240 +3V_PMU_RESET	TRUE			29 33

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6537	B
SCALE NONE	SHT 39 OF 44	

REVISION HISTORY

Proto Release

7/22/02 - Initial acquisition of schematic (from 051-6278 Rev 01)
Added P59 SO-DIMM connector as placeholder (p.12)
Added P59 LVDS connector as placeholder (p.22)
Changed J9 to 10 pin Elco connector for modem (p.25)
Changed PBUS holdup caps to P59 electrolytic cans (p.30)
7/23/02 - Removed L3 (p.8)
Replaced processor with 360 pin Apollo (p.5,6)
7/24/02 - Added FETs between battery and PBUS rails for airline power (p.29)
8/10/02 - Added USB 2.0 (p.18)
8/20/02 - Removed spare pullup straps for Intrepid (p.9)
Removed USB overcurrent protection [to be placed on other boards] (p.18)
Changed right USB board connector to 16 pin Hirose connector (p.26)
Changed LIO board connector to 40 pin Molex connector (p.26)
Added 6 bypass caps to MAXBUS_SLEEP and CPU_VCORE_SLEEP (p.5)
8/26/02 - Removed 32 bypass caps for +3V_MAIN at Intrepid (p.16)
Removed 5 bypass caps for +2.5V_MAIN at Intrepid (p.16)
Removed 3 bypass caps for +1.5V_AGP at Intrepid (p.16)
Removed 4 bypass caps for MAXBUS_MAIN at Intrepid (p.16)
8/27/02 - Changed main battery connector to BP24067-R1, which is close to final (p.29)
8/29/02 - Added dedicated Boot Banger circuit (p.6)
Added 5 bypass caps to each SO-DIMM connector (p.11)
Added quad voltage circuit for bus slewing architecture (p.32)
8/30/02 - Changed to low profile 32.768kHz crystal for PMU (p.28)
Changed to Q11 adpater detection scheme (p.28)
9/03/02 - Corrected upper LVDS single pin nets (p.20)
Removed unintentional extra pulldown resistor at Intrepid (p.14)
9/17/02 - Numerous changes to stay in sync with P84 (all)
9/18/02 - Changed battery connector back to P84 part (p.29)
Added LMU circuitry to eliminate extra board (p.23)
Changed to P84 dual channel LVDS connector to reduce I2R cable losses(p.22)
9/19/02 - Removed unnecessary battery FETs [due to 3S only design] (p.29)
Modified chassis gnds on some components (all)
Removed LMU connector (p.23)
Corrected battery connector [same as P84] (p.29)
Removed P93 support (p.25)
Removed second fuse from FW ports [single fuse provides adequate power] (p.27)
9/23/02 - Replaced BCM5421 with Marvell 88E1111 (p.26)
Increased MAX_VIA_COUNT by two on most nets with this constraint for uVia (p.34,35)
9/27/02 - Corrected cpu, memory bus constraints to match manhattan lengths (p.34)
Swapped pins on L33, L35 for layout (p.31)
Changed Y6 to smaller form-factor crystal (p.26)
9/30/02 - Changed J19 (DC-in) to proper 4-pin connector (p.29)
Corrected holes and chassis gnds (p.4,all)
10/01/02 - Removed Intrepid 1.x specific circuitry (p.13)
10/03/02 - Numerous pin-swaps to accomodate board layout (all)
10/08/02 - Added page for functional test points (p.37)
10/09/02 - Changed 16 pin connectors (modem and right USB) to Foxconn parts (p.23)
10/10/02 - Clamped NEC NC pins high per documentation (p.17)
Added 10K pullup to CG_ADDRSEL and 10K pulldown to CG_FSEL on CY28512 (p.14)
Added SSCG/NO_SSCG stuffing options for CY28512 circuit (p.14)
Removed CPU_VGATE pullup to 5V to eliminate potential 3V/5V current path (p.32)
Removed Zebra 15/18 support per P84 (p.27)
Added second FW port power fuse (p.27)
Removed INT_CPUFB_IN cap per P84 (p.8)
Replaced IRF7822 FETs with IRF7811W in battery charger and 14V PBUS switchers (p.29,30)
Renamed optical interface for consistency (p.24,37)
Corrected PLL_CFG<4> for Apollo 7 [needs to always be zero] (p.5,7)
Removed temporary P84 constraints and finished up AGP clock changes (p.12,34)
Added stuffing options to power fans off 3V or 5V (p.25)
10/11/02 - Replaced DVI EMI caps with 0201 versions (p.22)
10/14/02 - Changed J18 to RJ45 with integrated magnetics (p.26)
10/15/02 - Moved Firewire connectors and port power switch to separate page (p.28)
Changed SMBus pullups to 7.15K, 1% as per iBooks/P84 [involved component net swaps] (p.29)
Added 0603 resistors as shorting pads for power up and reset (p.23)
Changed INT_MOD_SYNC, INT_MOD_DTI and INT_MOD_BITCLK to pulldowns per ERS [LA clk not used] (p.14)
Added damping resistor option to LMU crystal (p.23)
Changed INT_TST_PLEN_PD to pulldown only [LA clk not used] (p.13)
Changed JTAG_ENET_TDI to pullup [LA clk not used] (p.13)
Removed FW_LKON from Intrepid EXTINT3 [no longer used], pullup added (p.14)
Changed BBANG_HRESET_L pullup to 3V_SLEEP (p.6)
Changed FW_PC_PD, FW_PC_PU resistors to 5% (p.27)
Added 1K pulldown and net FW_PD2 to FW_PHY (p.27)
10/16/02 - Implemented new FW power switch and current limit (p.28)
Renamed +14V_PBUS to +PBUS (p.all)
Added A29 adapter detection circuit (p.29)
Added +PBUS current limiting circuit, removed battery charging current limit circuit (p.30)
Changed FW PHY pin DS1 to pullup to make Port 1 1394a only (p.27)
10/21/02 - Updated CY28512 clock chip to Rev B (p.14)
Changed keyboard ZIF to large SMK connector (p.23)
Added full support for non-zero CPU_PLL_CFG<4> in run state (p.7)
10/22/02 - Mirrored wireless connector for P59 flex (p.24)
10/23/02 - Changed LMU/sleep LED interface per p84 (p.23)
Changed LMU JTAG/I2C pinout/pullup/pulldown strategy per P84 (p.23)
Changed fan FETs to SI3446DV per P84 (p.25)
Pinned out audio connector (p.25)
Pinned out right USB connector (p.25)
Pinned out modem connector (p.25)
Added 2 functional test points to wireless connector (p.24,38)
Renamed FW low voltage power rails (p.27,37)
Renamed Vcore VID nets to be consistent with P84 (p.33)
Removed redundancy in DDR memory constraints (p.35)
10/24/02 - Changed FW DS2 strap to pullup to shut off port 2 (p.27)
Cleaned up CY28512B circuit as per P84 [powered off main, output divider and strap tweaks] (p.14)
Updated PCI clock series R values per P84 (p.12)
Changed power rail for ALS to +3V_MAIN per P84 (p.23)
Added 0 ohm short and bypass cap for GPU VDDVO per P84 (p.21,37)
Split FW_VGND into FW_VGND0 and FW_VGND1 (p.28,37)
Added TP nets to GPU for XOR-tree testing (p.19-21)
Changed fan PWM output pullups to +3V_SLEEP to prevent pump-up (p.25)
10/28/02 - Added FW thermal pad ground hole back in (p.27)
Repinned LMU pulldown for layout (p.23)
10/30/02 - Changed fan power rails to common net (p.25)
10/31/02 - Removed MLB ALS (p.23)
Added wireless RF_DISABLE_L pullup and AIRPORT_CLKRUN_L pulldown (p.24)
11/05/02 - Added 6 decoupling caps to CPU_VCORE_SLEEP (p.5)
Broke out quad OR-gate to discrete components for better placement (p.22,29)
11/06/02 - Changed 10 uF FW current limit output cap to two 4.7 uF caps (p.28)
Added 3 decoupling caps to CPU_VCORE_SLEEP (p.5)
Added 8 decoupling caps to each of +5V_MAIN and +3V_MAIN (p.32)
Removed XW17, jumper for CPU_VCORE_SLEEP (p.33)
Added decoupling cap to PMU reset OR gates (p.29)
11/08/02 - Changed Firewire PHY to Z17 (p.27)
Added bulk caps to fan connectors (p.25)
Added alternate chassis gnd connection for sleep LED (p.23)
11/11/02 - Removed +3V_MAIN option for P59 card (p.24)
11/13/02 - Removed LMU and associated circuitry (p.23)
11/21/02 - Implemented D3cold for all PCI devices (p.12,14,18)
11/25/02 - Renamed all components (all pages)
11/26/02 - Removed chokes from 1394b data pairs (p.27,28)

EVT RELEASE

12/13/02 - Added 12 pF caps to source of 33MHz PCI clocks since they can not be buried (p.12)
Replaced ADM1031 with ADT7460 [I2C Address Change!] (p.25)
Added ADT7460 hookups to GPU thermal diode (p.21,25)
Added FireWire B ESD protection circuits (p.28)
12/16/02 - Removed hole from FireWire ground pad (p.27)
DDR memory connector renamed to J25 (p.11)
12/20/02 - Removed LT4210 from FireWire port power (p.28)
Added F19,F20 as placeholders and experiment guides (p.28)
Added diodes to OR +5V_SLEEP into FW_PHY power supply (p.27)
12/26/02 - Updated CPU p/ns to production p/ns (p.5)
Removed RC glitch filter on CPU_DRDY_L (p.5,36)
Updated PCI source clock and internal spreading straps (p.8)
Changed BootROM PWD signal to INT_RESET_L per P84 (p.9)
Added CKE pulldowns per P84 (p.9)
Updated Ethernet series Rs per P84 [Clocks to 10 ohms, data to 22 ohms] (p.13)
Updated SSCG/NO_SSCG BOM options (p.14)
Renamed line-in and headphone sense lines to reflect active low signals (p.14,25.39)
Added 0 ohm Rs to make +5V_Intrepid rail hot or cold (p.15.16,38)
NO STUFFED ENTIRE +5V_LDO circuit (p.15)
Stuffed USB OCI_RC filters for 8 time constant [due to new port current limiters] (p.17)
Renamed USB OCI/PPON signals for left/right ports (p.17,39)
Updated GPU VCore to stay in sync with P84 [Jitter improvement] (p.20)
Added EMI caps to LVDS_DDC_CLK, INT_I2S0_SND_MCLK, INT_I2S0_SND_SCLK per P84 (p.22,25)
Added R800,R801 for eventual thermal diode in CPU (p.25)
Renamed R2000 to R799, R2001 to R802, R2002 to R803 (p.25)
Renamed F10 to F1, F20 to F2 [deleted old F1,F2] (p.28)
Added caps to FW ESD circuit that were missed (p.28)
Changed MAX4172 power source to save current on battery [per P84] (p.30)
Updated 1.5V/2.5V switcher BOM to stay in sync with P84 [FET change and current limits] (p.34)
Replaced all 13ZS1061 [1uF,0805,10V,20%] with 13ZS0046 [1uF,0603,10V,20%] (p.14,15,27,30,33,34)
Replaced all 13ZS0351 [1uF,0603,6.3V,10%] with 13ZS0046 [1uF,0603,10V,20%] (p.27,30)
01/02/03 - Updated FireWire fuse topology to that of P84 (p.28)
Updated system and power block diagrams (p.2,3)
01/03/03 - Corrected +2.5V_INTREPID connections to muxes and reference (p.9,10)
01/07/03 - Added NO_TEST nets to pads of DDR connector arms (p.11)
01/08/03 - Added 2N7002 circuits to ensure speakers are muted during power-up (p.25)
Changed R164 to 511 ohms to avoid low CPU clock amplitude (p.8)
01/09/03 - Added required pulldown to output of DVI HPD sense comparator (p.22)
Swapped R443 and R444 values to ensure Vgs < -4.5V (p.28)
Updated S-video filter values to those of P84 (p.22)
01/10/03 - Z77,Z723,Z761,Z776,Z789,Z787,Z722,Z738,Z760,Z742 & Z717 are changed to HOLE-VIA-20R10 (p.4)
01/13/03 - Add L53, L54, L55 for TMDS Data<0:2> Diff Pair (p.22)
01/14/03 - Add C812 - C821 (Total 10 0.22uF caps) for 2.5V Intrepid Decoupling (p.16)
Add C822 & C823 at Wireless Card connector MAIN_RESET_L & RF_DISABLE_L_SPN (p.24)
Change MATCHED_DELAY to 50 for all TMDS DIFF PAIR (p.37)
Change MATCHED_DELAY to 50 for all TMDS DIFF PAIR (p.37)
Add R810 & R811 for ALWAYS-ON FANs in Acrylic Build (p.25)
01/28/03 - Remove XW31/17 components (p.19-21)
Add M10 (p.19-21)
02/07/03 - Add Power Net Constraints for M10 (p.38)
Replace Singing PBUS Cap C49,C50,C67,C68,C80,C81,C95,C96,C108,C109,C120,C121 with 12GS0035 (for alt. 12GS0036) (p.33)
02/11/03 - Add FW Power Net Constraints (p.38)
Change signal constraints for AGP signals (p.36)
Add LMU connector and components (p.23)
Edit I2C table for LMU (p.13)
Change R500 to 19.6K (p.14)
Connect Clock Slewing RESET# to MAIN_RESET_L (p.14)
Change Ferrite Bean of ATI power supply to correct values (p.21)
Remove C141 PBUS CAP (p.31)
02/12/03 - Change and Rotate Keyboard Connector (p.23)
Add ATI Power sequencing Circuit for M10 Power-up and Power-down (p.19-22, p.32-35)

EVT RELEASE (continue)

02/13/03 - Add C825 (p.30)
02/17/03 - Rename all Reference Designators

EVT ENCLOSURE RELEASE

03/13/03 - Change 3-P FAN connectors to 4-P (p.25)
Add PU at PMU_SLEEP_LED_L for LMU (p.23)
Change stuffing option for clock slewing & PLL5 (p.14)
Change ATI M10 GPIO8 to Pull-down (p.20)
Remove Memory MoUx Ooms Resistors (p.10)
03/28/03 - Due to MLB outline change at DVI connector, CHGND1 has to be splitted into CHGND1 & CHGND2 (P 4 & 22)
Separate +3V and +5V traces running from 3/5V supply to 40Pin LIO connector (P 25 & 32)
R601 change from 100K to 4.7K (P 29)
Change airline detect to 13.1V or greater, R40 and R690 to 97.6K ohm (P 30 & 31)
Add C826 at U3 RS- pin (P 30)
Change D3 to 1N914 PN Junction Diode(P 31)
03/31/03 - Change AGPTEST Pull-up to 47ohm (it was 40ohm) (P 20)
Add circuits to prevent start-up Headphone POP (P 25)
Change all 1210 4.7uF to 1206 4.7uF Cap (13ZS0531) (various pages)
Modify FAN circuit to PWM active low signal (P25)
04/08/03 - Add SOFT_MODEM_support (P 14 & 25)
Add 10-Pin ELCO connector for Serial Debug Interface (P 25)
Change Q7 from SI4435DY to SUD45P03-10 (P 30)
Remove D34 RS3AB (P 30)
04/11/03 - Change FW Schottky Diode to a 3A part 37ZS0159 (P 28)
Change PBUS L69 and VCORE L71 Inductor (P 31 & 33)
Change C643 10uF Cap to 1206 package part (P 28)
Change all 6 VCORE Caps to 220uF Al Poly Cap 12ZS0024 (P 33)
Add Mitsumi MM1571J regulator to provide 1.8V TPVDD (P 21)
Change U34 to Mitsumi MM1571J part for ATI PLL 1.8V rail(P 21)
04/16/03 - Add FW Port ShutDown/PowerOn Circuit (P 28)
Change the I2C Pull-up for Sound/Modem to 1K ohm (P 14)
04/17/03 - Change 3V/5V inductors (152S0137) L61 & L62 (P 32)
04/21/03 - Add 12 ICT JTAG TEST PADs (P 39)
04/23/03 - Invert ATI GPIO15 signal, no stuff pull-up resistor (P 20)
Combine Q35 and Q36 into a Dual Package Part (P 22)
SWAP the ADT7460 Temperature Sense pair (P 25)
Change FW PHY to production part (P 26)
04/24/03 - Remove +3V_CBUS_SLEEP and US, use +3V_SLEEP directly (P 14,18,24)
Add 0402 Res between ATI PVDD/TPVDD rail and 10uF caps for stability purpose (P 21)
Add 90ohm common mode choke at TMDS data <0..2> pairs (P 22)
Add Sense Resistor to Vcore power rail, remove one 220uF cap <back to EVTA design> (P 33)
04/25/03 - Change C826 to 0.01uF 50V Cap (P 30)
04/30/03 - No stuff R676 to prevent +3V rail leakage (P 33)
05/02/03 - L45,L46,L47 is using Common Mode Choke TDK ACM2012D Part, will replace with ACM2012H Part if available (P 22)

DVT RELEASE

05/21/03 - Swap +PBUS and +24V_PBUS at Backup Battery Connector - J16 (P.31)
05/27/03 - Change RP31 to 4.7K for I2c timing specification (P.13)
Change Q62 & Q65 to SI7408DP part (P.33)
Change Q60, Q63 & Q66 to IRF7832 part and split C102 into 3 10pF caps (P.33)
Enable VCore Burst(Skip) Mode by no stuffing R67 (P.33)
Enable 3V/5V Burst Mode by changing R406 & R407 to 100K ohm (p.32)
Change Q68 to SI7860DP part (P.20)
Enable GPUCore Burst Mode by changing R358 to 2.2 ohm, no stuffing R344 and stuffing R343 (P.20)
Reduce audible noise by changing LG4 to 152S0139 (P.20)
Add C838, C840, C839, C844 & C845 10pF caps near the power switchers FETs (p.20, 32 & 34)
Change PWM L Fan input (both L&R Fans) to +5V_SLEEP pull-up (p.25)
05/30/03 - Connect SLEEP_LED_DGND to digital ground instead of CHGND5 (P.23)
06/03/03 - Add CPU Core Voltage offset option circuit (P.33)
GPU Vcore on/off timimg (P.20)
06/05/03 - Change FW-B connector to 514S0058 with internal shield pins (P.28)
06/06/03 - Add four 0ohm jumper, in case there is no sw support for the multi-stage VCore (P.38)
Change the +2.5V sleep FET to reduce Voltage drop on the rail (P.34)
06/12/03 - Change CBUS & USB2 REQ LINE Pullup to +3V_MAIN (P.12)
Add 0 ohm at USB AVSS GND (P.17)
Change TMDS common mode choke to TDK AMC2012-900H part (P.22)
Change HD_DMACK_L pullup R213 to 10K (P.24)
Add C847, C851 & C852 at ENET CLK for EMC (P.13 & 26)
Change Q34 to FDS3672 (P.28)
Change Q82 pin#4 connection to system digital GND (P.33)
Add C848 150uF cap at J3 for +5V_MAIN USB2 power (P.25)
Add C853 1000pF cap at Q64 (P.30)
Add RC at ADT7460 power rail for noise isolation (P.25)
Isolate THERM# signal at ADT7460 by using double inverters for THERM_L_OC (p.25)
Remove redundant pullup R601 for THERM_L_OC (P.29)
Remove SH2 EMI spring at CHGND5 (P.23)
Add additional PWR/GND pins at J17 for R-USB board (P.25)
06/13/03 - New SODIMM connector with 4 through-hole mounting pins (P.11)
Change CPU config stuffing option at R63 and R64 (P.7)
Stuff R288 for Cypress CIR chip (P.14)
Move CBUS_PCI_REQ_L back to +3V_SLEEP rail pull-up (P.12)
Change the TMDS Termination Resistor values to 162ohm (P.20)
Connect C847 at R160.1 (P.13)
Add 1000pF caps at ADT7460 D_plus/minus pairs (P.25)
Add SI1182 DVI transmitter to prevent leakage from DVI connector to the system (p.19&20)
06/16/03 - Replace C705,C707,C711,C703 & C685 with part 12ZS0025 (P.20&32)
Remove R271 0ohm resistor (P.34)
Edit Signal Constraints for TMDS routing and ENET routing (P.36&37)

DVT2 RELEASE

07/06/03 - Change R97 & R98 to 0402 package (P.33)
No Stuff R835 (P.19)
Change R198 to 100K ohm resistor (P.23)
Add Common Mode Choke L77 & L76 at FWB pairs (P.28)
Removed current monitoring IC for firewire port power (P.28)
Changed RP52,RP53,RP56,RP57 to 22ohm for EMI (P.19)

PRODUCTION RELEASE

07/28/03 - Change BOM option for C51,C52,C77,C78,C91,C92,C111 to 8.2uF Panasonic AL cap only (p. 34)
08/05/03 - Change +3V/5V ITH compensation and No-Stuff Feed Forward Caps (p. 32)
Change CPU VCORE setting for both BEST and BETTER configurations (p. 33)
08/07/03 - Change CPU VCORE setting for both BEST and BETTER configurations again (p. 33)

PRODUCTION RELEASE (2)

09/02/03 - Schematic 051-6537 cloned from 051-6338
09/03/03 - Remove XW Jumpers for production board
Change CPU VCORE setting and remove un-used MUX (U15) and un-used discretes (p 33)
Stuff R794, R795, R796 & R797 0ohm resistors (p 33)
09/04/03 - Change R611 to 511 ohm resistor to reduce sleep LED brightness (p 23)

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SIZE	DRAWING NUMBER	REV.
D	051-6537	B
SCALE NONE	SHT 40 OF 44	

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*** Signal Cross-Reference for the entire design ***

+1_0V_MARVELL     26D2< 38B3>
+1_5V_AGP         12B5< 12D1< 12D4< 15D5< 16C8<
                19C6< 19D6< 20A8< 20B4<> 20D5<>
                21B8< 21D6< 38C3>
+1_5V_AGP_GPU     21C5< 38C3>
+1_5V_AGP_NECK    20B4<> 38B3>
+1_5V_GPU_VDD15   20D3< 38C3>
+1_5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 38D3>
+1_5V_INTREPID_PLL1  14C3< 38D3>
+1_5V_INTREPID_PLL2  14D3< 38D3>
+1_5V_INTREPID_PLL3  14D3< 38D3>
+1_5V_INTREPID_PLL4  14D3< 38D3>
+1_5V_INTREPID_PLL5  12D3< 38D3>
+1_5V_INTREPID_PLL6  12D6< 38D3>
+1_5V_INTREPID_PLL7  8D5< 38D3>
+1_5V_INTREPID_PLL8  14D3< 38C3>
+1_5V_LDO         38D6>
+1_5V_MAIN        38D6>
+1_5V_SLEEP       38D6>
+1_5V_SLEEP_NECK  34D2<> 38B3>
+1_5V_SLEEP_VIN   38D6>
+1_8V_ATI_PVDD    20C5<> 21B6< 21B6< 21D6<> 38C3>
+1_8V_ATI_TPVDD   21D1<> 38B3>
+1_8V_GPU         19A8< 19C2< 20D7< 21A2< 21A6<
                21B1< 21B6< 21C8< 21D6< 21D8< 38C3>
+1_8V_GPU_AVDD    21D5< 38B3>
+1_8V_GPU_AVDDQ   21D4< 21D7< 38B3>
+1_8V_GPU_DVO     21B2<
+1_8V_GPU_MEMPLL  21B5< 38B3>
+1_8V_GPU_PLL     21D5< 38C3>
+1_8V_GPU_PNLIO   21A5< 38B3>
+1_8V_GPU_PNLPLL  21B5< 38B3>
+1_8V_GPU_TP_PLL  21B5< 21D1< 38B3>
+1_8V_GPU_VDDDI   21C7< 21D4< 38C3>
+1_8V_MAIN        38D6> 39C6>
+1_8V_PVDD_NECK   20B5<> 38B3>
+1_8V_SLEEP       38D6>
+1_8V_SLEEP_NECK  34D2<> 38B3>
+1_95V_FW_DVDD    27C4< 27C7<> 27D5< 38A3>
+1_95V_FW_DVDD_PORT1  27D6< 38A3>
+1_95V_FW_DVDD_RX0  27C5< 38A3>
+1_95V_FW_DVDD_TX0  27C5< 38A3>
+1_95V_FW_PLL400VDD  27C4< 38A3>
+1_95V_FW_PLL500VDD  27D4< 38A3>
+1_95V_FW_PLLVDD  27D4< 27D6<> 38A3>
+2_5V_CG_MAIN     14C6<
+2_5V_GPU         21A7<> 21B6< 21C6< 21C8< 21D8<
                38C3>
+2_5V_GPU_A2VDD   21D4< 21D7< 38B3>
+2_5V_GPU_MCLK    21C7< 21D4< 38B3>
+2_5V_GPU_MEMCORE  21C5< 38C3>
+2_5V_GPU_PNLIO   21A5< 38C3>
+2_5V_INTREPID    9A7< 10D3< 10D5< 10D6< 10D8< 15D6<
                16B8< 38D3>
+2_5V_MAIN        38D6> 39C6>
+2_5V_MARVELL     26B8< 26C4<> 38B3>
+2_5V_MARVELL_AVDD  26C4< 38B3>
+2_5V_SLEEP       38D6>
+2_5V_SLEEP_NECK1  20C4<> 38B3>
+2_5V_SLEEP_NECK2  34D2<> 38B3>
+3V_AIRPORT       38C3> 39C3>
+3V_ATI_OSC_SLEEP  19B2< 38B3>
+3V_ATI_SS        19A3< 38B3>
+3V_CG_PLL_MAIN   14C6<
+3V_FW            27A3< 27D7<> 28D5<> 38A3>
+3V_FW_AVDD       27C6< 38A3>
+3V_FW_AVDD_PORT0  27C6< 38A3>
+3V_FW_AVDD_PORT1  27C6< 38A3>
+3V_FW_AVDD_PORT2  27D6< 38A3>
+3V_FW_ESD        28B4<> 28D3<>
+3V_FW_ESD_ILIM   28D4<
+3V_FW_UF         27D7<> 38A3>
+3V_GPU           12D1< 19B8< 19C6< 19C8< 19D6<
                20C4< 20C5< 20C7< 20D7< 21A6< 21B1<
                38C3>
+3V_GPU_FLT       21B2< 38C3>
+3V_HALL_EFFECT   23B4<> 38B6> 39B3>
+3V_INTREPID_USB  14C3< 38D3>
+3V_LCD           22B4<> 38B6> 39B6>
+3V_LCD_SW        22B4<> 38B6>
+3V_MAIN          23B7<> 38D6> 39C6>
+3V_MAIN_AUD      25C6<> 32C1<> 38B6>
+3V_NEC_VDD       17B3< 17D7< 17D7< 38A3>
+3V_PMU           38D6> 39C6>
+3V_PMU_AVCC      25B1< 29B6< 29D5<> 38C6>
+3V_PMU_ESR       31A2< 38C6>
+3V_PMU_RESET     29B7< 33A4<> 39C1>
+3V_SI_AVCC       19D3<
+3V_SI_PLLVCC     19D3<
+3V_SI_VCC        19D3<
+3V_SLEEP         38D6> 39A6> 39B6>
+3V_SLEEP_NECK    34D1<> 38B3>
+3V_SLP_OK_L      32B4<>
+3V_SLP_ON        32A5<>
+4_6V_BU          31B3<> 32B7< 38C6>
+4_85V_ESR        31A4< 38C6>
+4_85V_RAW        29A5< 31B4<> 38C6>
+5V_DDC_SLEEP     22D3<> 22D5<> 38B6> 39B6>
+5V_DDC_SLEEP_UF  22D6< 38B6>
+5V_HD_SLEEP      24D1<> 32A7<> 38C6>
+5V_INV_SW        22B2<> 38B6> 39A6>
+5V_INV_UF_SW     22B2<> 38B6>
+5V_MAIN          38D6> 39A6> 39C6>
+5V_MAIN_AUD      25C6<> 32C8<> 38B6>
+5V_SLEEP         38D6> 39A6> 39C6>
+5V_TPAD_SLEEP    23B5<> 38B6> 39B3>
+14V_INV          22B2<> 38B6> 39B6>
+24V_PBUS         38D6> 39C6>
+ADAPTER          30D8<> 31A7< 38C6> 39D1>
+ADAPTER_ILIM     31A6< 38C6>
+ADAPTER_OR_BATT  31A5<> 38C6>
+ADAPTER_SENSE    30D4<> 38C6>
+ADAPTER_SW       30D5<> 38C6> 38C6>
+BATT             38D6>
+BATT_14V_FUSE    30D1<> 38C6>
+BATT_24V_FUSE    30B1< 30D2<> 38C6>
+BATT_POS         30A4<> 38C6> 39A3>
+BATT_RSNS        30B2< 38C6>
+BATT_VSNS        30A4< 38C6>
+FAN_PWR          25A3< 25A4< 38B6> 39A3>
+FW_AMP_SENSE     38A3>
+FW_PBUS          28D7<> 38A3>
+FW_PWR1          28C5< 38A3>
+FW_PWR_OR        27B8< 27D8<> 28D5<> 38A3>
+FW_SW            28D5<> 38A3>
+FW_VP0           28C1<> 38A3> 39A3>
+FW_VP1           28A3<> 38A3> 39D1>
+GPU_VDD15_NECK   20B5<> 38B3>
+GPU_VDD15_UF     20B5<> 20D4<> 38B3>
+HD_LOGIC_SLEEP   24C2<> 38C6>
+PBUS             38D6> 39C6>
+VCC_CBUS_SW      18B1<> 18B2<> 18D2<> 38C3>
+VPP_CBUS_SW      18B1<> 18B2<> 18D2<> 38C3>
1V20_REF          30C7< 31C8< 38D1>
1V65_REF          30A5<
1_5V_BOOST        34C6<> 38C1>
1_5V_BST          34C5<> 38C1>
1_5V_DH           34C5<> 38C1>
1_5V_DL           34B5<> 38C1>
1_5V_FB           34B5< 34B7< 38C1>
1_5V_ILIM         34C5<> 38C1>
1_5V_LX           34B5<> 38C1>
1_5V_SLEEP_EN_L   34C7<> 34D7<>
1_8V_PVDD_STD     21D6<
1_8V_SLEEP_PWREN_L  34A3<>
1_8V_SW           34A5<> 38A1>
1_8V_TPVDD_STD    21D1<
1_8V_VFB          34A5<> 38A1>
2_5V_BOOST        34C4<> 38D1>
2_5V_BST          34C4<> 38D1>
2_5V_DH           34C4<> 38D1>
2_5V_DL           34B4<> 38C1>
2_5V_ILIM         34C5<> 38C1>
2_5V_LX           34B4<> 38D1>
2_5V_SLEEP_PWREN_L  34C2<>
3V_5V_OK          32B4<> 34A8< 34D6<
3V_BG             32C4<>
3V_BOOST          32C4<>
3V_BOOST_ESR      32D3<>
3V_ITH            32C4<>
3V_ITH_RC         32C3<
3V_PMU_VTAP       31B3<
3V_RSNS           32D2< 38D1>
3V_RUNSS          32C4<
3V_SLEEP_PWREN_L  32B3<>
3V_SNSM           32C4< 37A2>

3V_SNSP           32C4< 37A2>
3V_SW             32C4<> 38D1>
3V_TG             32D4<>
3V_VOSNS          32C4<>
5V_BG             32C5<>
5V_BOOST          32C5<>
5V_BOOST_ESR      32D6<>
5V_HD_PWREN       32A8<>
5V_ITH            32C5<>
5V_ITH_RC         32C6<
5V_RSNS           32D7< 38D1>
5V_RUNSS          32C5<
5V_SLEEP_PWREN    32A8<>
5V_SNSM           32C5< 37A2>
5V_SNSP           32C5< 37A2>
5V_SW             32C5<> 38D1>
5V_TG             32C5<>
5V_VOSNS          32C5<>
1625_BG           31C5<>
1625_BST          31C5<
1625_BST_ESR      31C5<>
1625_COMP         30D2< 31C6<
1625_DIV          31C8<
1625_ENABLE       31D7<>
1625_ENABLE_L     31D6<>
1625_EXTVCC       31D5<> 38D1>
1625_FCB          31C6<
1625_INTVCC       31C5<> 38D1>
1625_RUNSS        31C6<
1625_SGND         31B7<> 38D1>
1625_TG           31C5<>
1625_VFB          31B5<>
1625_VIN          31C6< 38D1>
1625_VSW          31C4<> 38D1>
1772_ACIN         30B5<
1772_ACOK_L       30B5<> 30C4<>
1772_BST          30B4<>
1772_BST_ESR      30C3<
1772_CCI          30B5<>
1772_CCS          30B5<
1772_CCV          30B5<>
1772_CCV_RC       30B5<
1772_CELLS        30B4<
1772_CLS          30A4<
1772_CSIN         30B4<> 37A2>
1772_CSIP         30B4<> 37A2>
1772_CSSN         30C5< 37A2>
1772_CSSP         30C5< 37A2>
1772_DCIN         30B5< 38C6>
1772_DHI          30B4<>
1772_DLO          30B4<>
1772_DLOV         30B4<> 38C6>
1772_GND          30A5<> 38C6>
1772_ICHG         30B5<>
1772_ICTL         30B5<>
1772_IINP         30B5<
1772_LDO          30C4<> 38C6>
1772_LX           30B4<> 38C6>
1772_REF          30B5<>
1772_VCTL         30B5<
1778_BG           20A5<> 38B1>
1778_BST          20A5<> 38B1>
1778_BST_RC       20A5< 38B1>
1778_FCB          20A6< 38B1>
1778_GND          20A6< 20A7<> 38B1>
1778_ION          20A5< 38B1>
1778_ITH          20A6<> 38B1>
1778_ITH_RC       20A7< 38B1>
1778_SHDN_L       20A6<>
1778_TG           20A5<> 38B1>
1778_VCC          20A5< 38B1>
1778_VFB          20A2< 20A5< 38B1> 39C6>
1778_VIN          20A5< 38B1>
1778_VRNG         20A6< 38B1>
3405_MODE         26D5<
3405_VFB          26D4<>
3707_FCB          32C5<
3707_FSET         32C5<
3707_INTVCC       32D4<> 38D1>
3707_SGND         32B5<> 38D1>
3707_STBY         32C5<>
A29_CLS_ADJ       30A5<>
A29_CURRENT_ADJ   30C4<>
A29_DETECT        29A2< 30A5<> 30C4<>
A29_DET_L         29A3<
A29_DET_REF       29A4<
AC_DIV            30C7<
AC_ENABLE_GATE    30D6<>
AC_ENABLE_L       30C5<>
AC_GTR_18V        30C3<>
AC_IN             26B8<> 28C8< 29B3< 30C5<> 30C6<>
AC_IN_FW_CNTL     28C7<>
AC_IN_L           30C2<> 30C6<>
AC_IN_L_RC        30C2<>
ADAPTER_DET       25D8<> 29A4< 39A6>
ADAPTER_I_REG     30D3<>
ADT7460_ADR_ENABLE_L  25B3<>
ADT7460_TACH3_TP  25B3<
ADT7460_THERM_L   25B2<> 25B3<>
ADT7460_VCC       25C4<
ADT7460_VCORE_MON  5C8<> 25B4<>
AGP8X_DET_PU      19C6<>
AGP_AD<0>         12D2<> 19C7<>
AGP_AD<15..0>     37D5>
AGP_AD<1>         12C2<> 19C7<>
AGP_AD<2>         12C2<> 19C7<>
AGP_AD<3>         12C2<> 19C7<>
AGP_AD<4>         12C2<> 19C7<>
AGP_AD<5>         12C2<> 19C7<>
AGP_AD<6>         12C2<> 19C7<>
AGP_AD<7>         12C2<> 19C7<>
AGP_AD<8>         12C2<> 19C7<>
AGP_AD<9>         12C2<> 19C7<>
AGP_AD<10>        12C2<> 19C7<>
AGP_AD<11>        12C2<> 19C7<>
AGP_AD<12>        12C2<> 19C7<>
AGP_AD<13>        12C2<> 19C7<>
AGP_AD<14>        12C2<> 19C7<>
AGP_AD<15>        12C2<> 19C7<>
AGP_AD<16>        12C2<> 19C7<>
AGP_AD<31..16>    37D5>
AGP_AD<17>        12C2<> 19C7<>
AGP_AD<18>        12C2<> 19C7<>
AGP_AD<19>        12C2<> 19C7<>
AGP_AD<20>        12C2<> 19C7<>
AGP_AD<21>        12C2<> 19C7<>
AGP_AD<22>        12C2<> 19C7<>
AGP_AD<23>        12C2<> 19C7<>
AGP_AD<24>        12C2<> 19C7<>
AGP_AD<25>        12C2<> 19C7<>
AGP_AD<26>        12C2<> 19D7<>
AGP_AD<27>        12B2<> 19D7<>
AGP_AD<28>        12B2<> 19D7<>
AGP_AD<29>        12B2<> 19D7<>
AGP_AD<30>        12B2<> 19D7<>
AGP_AD<31>        12B2<> 19D7<>
AGP_AD_STB<0>     12A2<> 12B2< 19D6<> 37D5>
AGP_AD_STB<1>     12A2<> 12B2< 19D6<> 37D5>
AGP_AD_STB_L<0>   12A2<> 12B2< 19D6<> 37D5>
AGP_AD_STB_L<1>   12A2< 12A2<> 19D6<> 37D5>
AGP_ATI_INT_L     14B5<> 19B7<>
AGP_ATI_RESET_L   19B7<
AGP_ATI_VREF      19B7<
AGP_ATI_VREFG     19B7<
AGP_BUSY_L        12C4<> 12D2< 19D6>
AGP_CBE<0>        12B2<> 19B7<>
AGP_CBE<1..0>     37D5>
AGP_CBE<1>        12B2<> 19B7<>
AGP_CBE<2>        12B2<> 19B7<>
AGP_CBE<3..2>     37D5>
AGP_CBE<3>        12B2<> 19B7<>
AGP_DEVSEL_L      12B2<> 12C2< 19B7<> 37D5>
AGP_FRAME_L       12B2<> 12C2< 19B7<> 37D5>
AGP_GNT_L         12C2< 12D2<> 19B7< 37D5>
AGP_IRDY_L        12B2<> 12C2< 19B7<> 37D5>
AGP_PAR           12B2<> 19B7> 37D5>
AGP_PIPE_L        12A2<> 12B2<
AGP_RBF_L         12A2<> 12C2< 19C6> 37C5>
AGP_REQ_L         12C2< 12D2<> 19B7<> 37D5>
AGP_SBA<0>        12B2< 19C6>
AGP_SBA<7..0>     37D5>
AGP_SBA<1>        12B2<> 19C6>
AGP_SBA<2>        12B2<> 19C6>
AGP_SBA<3>        12B2<> 19C6>
AGP_SBA<4>        12B2<> 19C6>
AGP_SBA<5>        12B2<> 19C6>
AGP_SBA<6>        12B2<> 19C6>
AGP_SBA<7>        12B2<> 19C6<>

AGP_SB_STB        12B2< 12B2<> 19C6<> 37D5>
AGP_SB_STB_L      12A2< 12A2<> 19C6<> 37D5>
AGP_ST<0>         12A2<> 19C6<
AGP_ST<1>         12A2<> 19C6<
AGP_ST<2>         12A2<> 19C6<
AGP_STOP_L        12B2<> 12C2< 19B7<> 37D5>
AGP_STP_L         19C6<
AGP_SUS_STAT_L_PU  19C6<
AGP_TRDY_L        12B2<> 12C2< 19B7<> 37D5>
AGP_WBF_L         12A4<> 12B2< 19B7>
AIRPORT_CLKRUN_L  24C6<> 39C3>
AIRPORT_IDSEL     24C5<>
AIRPORT_PCI_GNT_L  12D7<> 24D5<> 39C3>
AIRPORT_PCI_INT_L  14B5<> 14D7< 24D5<> 39C3>
AIRPORT_PCI_REQ_L  12A7< 12D7<> 24D6<> 39C3>
ATI_AGP_FBSKEW<0>  20C2< 20C7<>
ATI_AGP_FBSKEW<1>  20C2< 20C7<>
ATI_BUS_CFG<0>    20B2< 20C7<>
ATI_BUS_CFG<1>    20B2< 20C7<>
ATI_BUS_CFG<2>    20B2< 20C7<>
ATI_CLK27M_IN     19A2< 20B7< 35B1>
ATI_CLK27M_OSC    19A2< 35B1>
ATI_CLK27M_OSC_SS  19A1< 19A4< 35B1>
ATI_DBI_HI_PU     19C6<>
ATI_DBI_LO_PU     19C6<>
ATI_DVOD<0>       19B4< 20D7<>
ATI_DVOD<11..0>   36C1>
ATI_DVOD<1>       19B4< 20D7<>
ATI_DVOD<2>       19B4< 20D7<>
ATI_DVOD<3>       19B4< 20D7<>
ATI_DVOD<4>       19B4< 20D7<>
ATI_DVOD<5>       19B4< 20D7<>
ATI_DVOD<6>       19B4< 20D7<>
ATI_DVOD<7>       19B4< 20D7<>
ATI_DVOD<8>       19B3< 20D7<>
ATI_DVOD<9>       19B3< 20D7<>
ATI_DVOD<10>      19B3< 20D7<>
ATI_DVOD<11>      19B3< 20D7<>
ATI_DVOD_DE       19B3< 20C7<> 36C1>
ATI_DVOVMODE      21A3<
ATI_DVO_CLKP      19B3< 20C7<> 36C1>
ATI_DVO_HSYNC     19B3< 20C7<> 36C1>
ATI_DVO_VSYNC     19B3< 20C7<> 36C1>
ATI_GPIO7_SPN     20C7<>
ATI_GPIO8_PD      20C7<>
ATI_GPIO9_SPN     20C7<>
ATI_GPIO10_SPN    20C7<>
ATI_GPIO11_SPN    20C7<>
ATI_GPIO12_SPN    20C7<>
ATI_GPIO13_SPN    20C7<>
ATI_HSYNC         20D5<> 22D8<
ATI_HSYNC_BUF     22D8<>
ATI_MEMTEST       19A6<>
ATI_MEMVMODE0     19A7<
ATI_MEMVMODE1     19A7<
ATI_OSC_OE        19A3<
ATI_PVDD_BYP      21D6<>
ATI_R2SET         20D6<>
ATI_RSET          20D6<>
ATI_RSTB_MSK      19C6<>
ATI_SSCLK_IN      19A2< 20B7<> 35B1>
ATI_SSCLK_UF      19A2<> 35B1>
ATI_TESTEN        20B7<
ATI_TMDS_CLKN     20B7> 20B8< 37B2>
ATI_TMDS_CLKP     20B7> 20B8< 37B2>
ATI_TMDS_DN<0>    20B7< 20B7> 37B2>
ATI_TMDS_DN<1>    20B7> 20B8< 37B2>
ATI_TMDS_DN<2>    20B7< 20B7> 37B2>
ATI_TMDS_DP<0>    20B7< 20B7> 37B2>
ATI_TMDS_DP<1>    20B7> 20B8< 37B2>
ATI_TMDS_DP<2>    20B7< 20B7> 37B2>
ATI_TPVDD_BYP     21D1<>
ATI_VSYNC         20D5<> 22D8<
ATI_VSYNC_BUF     22D8<>
ATI_X1CLK_SKEW<0>  20C2< 20C7<>
ATI_X1CLK_SKEW<1>  20B2< 20C7<>
AUD_GND           25C8<> 38B6>
AUXWIN_PU         20C6<>
BATTV_HIGH        30B7<>
BATTV_LOW         30B8<>
BATT_14PBUS_EN    30C1<>
BATT_14V_GATE     30C1<>
BATT_24PBUS_EN    30C2<>
BATT_24V_GATE     30C1<>
BATT_CLK          30A4<> 39A3>
BATT_DATA         30A4<> 39A3>
BATT_DIV          30A5<
BATT_LOW          30A6<>
BATT_LOW_L        30B6<>
BATT_NEG          30A4<> 38C6> 39A3>
BBANG_HRESET_L    6A2< 6B3<>
BBANG_JTAG_TCK    6A4< 6B2<> 6C2<
BBANG_TCK_EN      6A4<
BB_EEPR_ADDR      6C2< 6D3<
BB_EEPR_WP_PD     6D2<>
BB_MISO           6B3<> 6C2<
BB_MOSI           6B3<> 6C2<
BB_RESET_L        6C3< 39C1>
BB_SCK            6B3<> 6C2<
BB_XTAL1_SPN      6C3<>
BFR_TDO           6C2< 6C2<>
BKFD_PROT_EN_L    30C5<>
BKFD_PROT_GATE    30D5<>
BRIGHT_PWM        22A2<> 39A6>
BRIGHT_PWM_UF     22A2<>
BT_USB_DM         14C1< 25D8<> 37B2> 39D3>
BT_USB_DP         14C1< 25D8<> 37B2> 39D3>
CAPSLOCK_LED      23C2<
CAPSLOCK_LED_L    23C3< 29C7<
CBUS_ADDR<0>      18B1<> 18B4>
CBUS_ADDR<1>      18B1<> 18B4>
CBUS_ADDR<2>      18B1<> 18B4>
CBUS_ADDR<3>      18B1<> 18B4>
CBUS_ADDR<4>      18B1<> 18B4>
CBUS_ADDR<5>      18B1<> 18B4>
CBUS_ADDR<6>      18B1<> 18B4>
CBUS_ADDR<7>      18B1<> 18B4>
CBUS_ADDR<8>      18B1<> 18B4>
CBUS_ADDR<9>      18B1<> 18B4>
CBUS_ADDR<10>     18B4> 18C1<>
CBUS_ADDR<11>     18B1<> 18B4>
CBUS_ADDR<12>     18B1<> 18B4>
CBUS_ADDR<13>     18B1<> 18B4>
CBUS_ADDR<14>     18B1<> 18B4>
CBUS_ADDR<15>     18B1<> 18B4>
CBUS_ADDR<16>     18B1<> 18B4<
CBUS_ADDR<17>     18B2<> 18B4>
CBUS_ADDR<18>     18B2<> 18B4>
CBUS_ADDR<19>     18B2<> 18B4>
CBUS_ADDR<20>     18B2<> 18B4>
CBUS_ADDR<21>     18B2<> 18B4>
CBUS_ADDR<22>     18A4> 18B2<>
CBUS_ADDR<23>     18A4> 18B2<>
CBUS_ADDR<24>     18A4> 18B2<>
CBUS_ADDR<25>     18A4> 18B2<>
CBUS_ADDR_16_UF   18B5<>
CBUS_BVD1_L       18A2<> 18C4<
CBUS_BVD2_L       18B2<> 18C4<
CBUS_CE1_L        18C1<> 18C4>
CBUS_CE2_L        18B2<> 18B4>
CBUS_DATA<0>      18A1<> 18A4<>
CBUS_DATA<1>      18A1<> 18A4<>
CBUS_DATA<2>      18A1<> 18A4<>
CBUS_DATA<3>      18A4<> 18C1<>
CBUS_DATA<4>      18A4<> 18C1<>
CBUS_DATA<5>      18A4<> 18C1<>
CBUS_DATA<6>      18A4<> 18C1<>
CBUS_DATA<7>      18A4<> 18C1<>
CBUS_DATA<8>      18A2<> 18A4<>
CBUS_DATA<9>      18A2<> 18A4<>
CBUS_DATA<10>     18A2<> 18A4<>
CBUS_DATA<11>     18A4<> 18C2<>
CBUS_DATA<12>     18A4<> 18C2<>
CBUS_DATA<13>     18A4<> 18C2<>
CBUS_DATA<14>     18A4<> 18C2<>
CBUS_DATA<15>     18A4<> 18C2<>
CBUS_DET_1_L      18C2<> 18C4< 39C6>
CBUS_DET_2_L      18A2<> 18C4< 39C6>
CBUS_INPACK_L     18B2<> 18B4<
CBUS_INT_L        14B5<> 14D7< 18A7<>
CBUS_IORD_L       18B2<> 18C4>
CBUS_IOWR_L       18B2<> 18C4>
CBUS_MFUNC1_PD    18A7<> 18A7<
CBUS_MFUNC2_PD    18A7<> 18A7<
CBUS_MFUNC3_PD    18A7<> 18A7<
CBUS_MFUNC4_PD    18A7<> 18A7<
CBUS_MFUNC5_PD    18A7<> 18A7<
CBUS_MFUNC6_PD    18A7<> 18A7<

CBUS_OE_L         18B1<> 18C4>
CBUS_PCI_GNT_L    12D7<> 18A7<
CBUS_PCI_IDSEL    18B7<
CBUS_PCI_REQ_L    12A7< 12D7<> 18A7>
CBUS_PCI_RESET_L  18A7<
CBUS_READY        18B1<> 18C4<
CBUS_REG_L        18B2<> 18C4>
CBUS_RESET_L      18B2<> 18C4>
CBUS_SUSPEND_PU   18A7< 18D7<
CBUS_VCCD0_L      18C4<>
CBUS_VCCD1_L      18C4<>
CBUS_VPPD0        18C4<>
CBUS_VPPD1        18C5<>
CBUS_VS1          18B2<> 18C4<>
CBUS_VS2          18B2<> 18C4<>
CBUS_WAIT_L       18B2<> 18B4<
CBUS_WE_L         18B1<> 18C4>
CBUS_WP_L         18A1<> 18B4<
CG_ADDRSEL        14B7<
CG_CLKOUT         14B6<>
CG_FSEL           14B7< 14C5<>
CG_LOCK           14B7<>
CG_RESET_L        14B7<
CHARGE_DISABLE    30A7<>
CHARGE_LED_L      25D8<> 29C6<> 29D7< 39A6>
CLK10M_PMU_XIN    29B6<
CLK10M_PMU_XOUT   29B6<
CLK10M_PMU_XOUT_UF  29B7<
CLK18M_INT_EXT    14B6<> 35B1>
CLK18M_INT_XIN    14A5< 35B1>
CLK18M_INT_XOUT   14A5<> 35B1>
CLK18M_XTAL_IN    14A5< 35B1>
CLK25M_ENET_XIN   26A7<>
CLK25M_ENET_XOUT  26A7<>
CLK25M_XTAL_IN    26A7<>
CLK32K_PMU_XIN    29B3<>
CLK32K_PMU_XOUT   29B3<>
CLK32K_PMU_XOUT_UF  29B2<>
CLK33M_AIRPORT    12D8< 24D5<> 35C1> 39C3>
CLK33M_AIRPORT_UF  12C7<> 35C1>
CLK33M_CBUS       12D8< 18A7< 35C1>
CLK33M_CBUS_UF    12C7<> 35C1>
CLK33M_NEC        12C8< 17B7< 35C1>
CLK33M_NEC_UF     12C7<> 35C1>
CLK66M_AGP_1_5V_TP  12C4>
CLK66M_GPU_AGP    12C8< 19B7< 35C1>
CLK66M_GPU_AGP_UF  12C7<> 35C1>
CLKENET_LINK_GBE_REF  13C5< 26C8< 35B1>
CLKENET_LINK_GTX  13C5<> 35A1>
CLKENET_LINK_RX   13D5< 26C8< 35B1>
CLKENET_LINK_TX   13D5< 26D8< 35A1>
CLKENET_PHY_GBE_REF  26C7<> 35B1>
CLKENET_PHY_GTX   13C6< 26C7< 35A1>
CLKENET_PHY_RX    26C7<> 35B1>
CLKENET_PHY_TX    26D7<> 35A1>
CLKFW_LINK_LCLK   13C3< 35A1>
CLKFW_LINK_PCLK   13C3<> 27C3< 35A1>
CLKFW_PHY_LCLK    13C2< 27B7< 35A1>
CLKFW_PHY_PCLK    27B4> 27C4< 35A1>
CLKLVDS_LN        20B5> 22A4<> 37C2> 39B6>
CLKLVDS_LP        20B5> 22A4<> 37C2> 39B6>
CLKLVDS_UN        20B5> 22A4<> 37C2>
CLKLVDS_UP        20B5> 22A4<> 37C2>
COMM_DTR_L        14C2< 25C1<> 39B3>
COMM_GPIO_L       14C2<> 25C2<> 39B3>
COMM_RESET_L      14C5<> 25D4<> 39B3>
COMM_RING_DET_L   14B5<> 14C7< 25C3<> 29C6<> 39B3>
COMM_RTS_L        14C2< 25C1<> 39B3>
COMM_RXD          14C2< 25C1<> 39B3>
COMM_SHUTDOWN     14C5<> 25D4<> 39B3>
COMM_TRXC         14C2<> 25C2<> 39B3>
COMM_TXD_L        14C2<> 25C2<> 39B3>
COMP_RC           31C6<
CPU_AACK_L        5A7< 8B5<> 8C2< 36D5>
CPU_ADDR<0>       5C7<> 8D5<>
CPU_ADDR<0..31>   36D5>
CPU_ADDR<1>       5C7<> 8D5<>
CPU_ADDR<2>       5C7<> 8D5<>
CPU_ADDR<3>       5C7<> 8D5<>
CPU_ADDR<4>       5C7<> 8D5<>
CPU_ADDR<5>       5C7<> 8C5<>
CPU_ADDR<6>       5C7<> 8C5<>
CPU_ADDR<7>       5C7<> 8C5<>
CPU_ADDR<8>       5C7<> 8C5<>
CPU_ADDR<9>       5C7<> 8C5<>
CPU_ADDR<10>      5B7<> 8C5<>
CPU_ADDR<11>      5B7<> 8C5<>
CPU_ADDR<12>      5B7<> 8C5<>
CPU_ADDR<13>      5B7<> 8C5<>
CPU_ADDR<14>      5B7<> 8C5<>
CPU_ADDR<15>      5B7<> 8C5<>
CPU_ADDR<16>      5B7<> 8C5<>
CPU_ADDR<17>      5B7<> 8C5<>
CPU_ADDR<18>      5B7<> 8C5<>
CPU_ADDR<19>      5B7<> 8C5<>
CPU_ADDR<20>      5B7<> 8C5<>
CPU_ADDR<21>      5B7<> 8C5<>
CPU_ADDR<22>      5B7<> 8C5<>
CPU_ADDR<23>      5B7<> 8C5<>
CPU_ADDR<24>      5B7<> 8C5<>
CPU_ADDR<25>      5B7<> 8C5<>
CPU_ADDR<26>      5B7<> 8C5<>
CPU_ADDR<27>      5B7<> 8C5<>
CPU_ADDR<28>      5B7<> 8C5<>
CPU_ADDR<29>      5B7<> 8C5<>
CPU_ADDR<30>      5B7<> 8C5<>
CPU_ADDR<31>      5B7<> 8C5<>
CPU_ARTRY_L       5A7<> 8B5<> 8D2< 36D5>
CPU_AVDD          5C3< 38D3>
CPU_BG_L          5C7< 8C2< 8D5<> 36D5>
CPU_BR_L          5C7> 8D2< 8D5< 36D5>
CPU_BUS_VSEL      5C3< 7A6<
CPU_CHKSTP_OUT_L  5B3<> 5C2< 39D6>
CPU_CHKS_L        5A3< 5D2<
CPU_CI_L          5A7> 8B5<> 36D5>
CPU_CLKOUT_SPN    5C3>
CPU_CLK_EN        8A5< 29C4<>
CPU_DATA<0>       6D8<> 8D3<>
CPU_DATA<0..31>   36D5>
CPU_DATA<1>       6D8<> 8D3<>
CPU_DATA<2>       6D8<> 8D3<>
CPU_DATA<3>       6D8<> 8D3<>
CPU_DATA<4>       6D8<> 8D3<>
CPU_DATA<5>       6D8<> 8D3<>
CPU_DATA<6>       6D8<> 8D3<>
CPU_DATA<7>       6D8<> 8D3<>
CPU_DATA<8>       6D8<> 8D3<>
CPU_DATA<9>       6C8<> 8D3<>
CPU_DATA<10>      6C8<> 8D3<>
CPU_DATA<11>      6C8<> 8D3<>
CPU_DATA<12>      6C8<> 8C3<>
CPU_DATA<13>      6C8<> 8C3<>
CPU_DATA<14>      6C8<> 8C3<>
CPU_DATA<15>      6C8<> 8C3<>
CPU_DATA<16>      6C8<> 8C3<>
CPU_DATA<17>      6C8<> 8C3<>
CPU_DATA<18>      6C8<> 8C3<>
CPU_DATA<19>      6C8<> 8C3<>
CPU_DATA<20>      6C8<> 8C3<>
CPU_DATA<21>      6C8<> 8C3<>
CPU_DATA<22>      6C8<> 8C3<>
CPU_DATA<23>      6C8<> 8C3<>
CPU_DATA<24>      6C8<> 8C3<>
CPU_DATA<25>      6C8<> 8C3<>
CPU_DATA<26>      6C8<> 8C3<>
CPU_DATA<27>      6C8<> 8C3<>
CPU_DATA<28>      6C8<> 8C3<>
CPU_DATA<29>      6C8<> 8C3<>
CPU_DATA<30>      6C8<> 8C3<>
CPU_DATA<31>      6C8<> 8C3<>
CPU_DATA<32>      6C8<> 8C3<> 8D8<
CPU_DATA<32..63>  36D5>
CPU_DATA<33>      6C8<> 8C3<> 8D8<
CPU_DATA<34>      6C8<> 8C3<> 8D8<
CPU_DATA<35>      6C8<> 8C3<> 8D8<
CPU_DATA<36>      6B8<> 8C3<> 8D8<
CPU_DATA<37>      6B8<> 8C3<> 8D8<
CPU_DATA<38>      6B8<> 8C3<> 8D8<
CPU_DATA<39>      6B8<> 8B3<> 8D8<
CPU_DATA<40>      6B8<> 8B3<> 8C8<
CPU_DATA<41>      6B8<> 8B3<> 8C8<
CPU_DATA<42>      6B8<> 8B3<> 8C8<
CPU_DATA<43>      6B8<> 8B3<> 8C8<
CPU_DATA<44>      6B8<> 8B3<> 8C8<
CPU_DATA<45>      6B8<> 8B3<> 8C8<
CPU_DATA<46>      6B8<> 8B3<> 8B8<
CPU_DATA<47>      6B8<> 8B3<> 8B8<
CPU_DATA<48>      6B8<> 8A8< 8B3<>

CPU_DATA<49>      6B8<> 8A8< 8B3<>
CPU_DATA<50>      6B8<> 8A8< 8B3<>
CPU_DATA<51>      6B8<> 8A8< 8B3<>
CPU_DATA<52>      6B8<> 8A8< 8B3<>
CPU_DATA<53>      6B8<> 8A8< 8B3<>
CPU_DATA<54>      6B8<> 8A8< 8B3<>
CPU_DATA<55>      6B8<> 8A8< 8B3<>
CPU_DATA<56>      6B8<> 8B3< 8B3<>
CPU_DATA<57>      6B8<> 8B3< 8B3<>
CPU_DATA<58>      6B8<> 8B3< 8B3<>
CPU_DATA<59>      6B8<> 8B3< 8B3<>
CPU_DATA<60>      6B8<> 8B3< 8B3<>
CPU_DATA<61>      6B8<> 8B3< 8B3<>
CPU_DATA<62>      6A8<> 8B3< 8B3<>
CPU_DATA<63>      6A8<> 8B3< 8B3<>
CPU_DBG_L         5C3< 8A3<> 8C2< 36D5>
CPU_DRDY_L        5C3> 8A3< 8C2< 36D5>
CPU_DTI<0>        5C3< 8A3<>
CPU_DTI<0..2>     36D5>
CPU_DTI<1>        5C3< 8A3<>
CPU_DTI<2>        5C3< 8A3<>
CPU_EDTI          5B2< 5C3<
CPU_EMODE0_L      5A3< 7A4<
CPU_EMODE1_L      5A3< 5C2<
CPU_GBL_L         5A7<> 8B5<> 36D5>
CPU_HIT_L         5A7> 8B5< 8D2< 36D5>
CPU_HRESET_INV    7A7<>
CPU_HRESET_L      5B3< 5C2< 6A1<> 7A5< 7A8< 39D6>
CPU_L1TSTCLK      5B2< 5B3<
CPU_L2TSTCLK      5B3< 5C2<
CPU_LSSD_MODE     5B3< 5C2<
CPU_MCP_L         5B3< 5D2<
CPU_PLL_CFG<0>    5C3< 7D3<
CPU_PLL_CFG<1>    5C3< 7D3<
CPU_PLL_CFG<2>    5C3< 7D3<
CPU_PLL_CFG<3>    5C3< 7D3<
CPU_PLL_CFG<4>    5C3< 7D3<>
CPU_PLL_CFGEXT    7D4<>
CPU_PLL_FS00      7C4<>
CPU_PLL_FS01      7C4<
CPU_PLL_FS10      7C4<
CPU_PLL_STOP_BASE  7C7<
CPU_PLL_STOP_OC   7C4<> 7C8<> 29B6<>
CPU_PMONIN_L      5A3< 5C2<
CPU_PULLDOWN      5A2< 5A3< 5A3< 5C7<>
CPU_PULLUP        5A3< 5C2<
CPU_QACK_L        5B3< 8B5<> 36D5>
CPU_QREQ_L        5B3> 8B5< 8C2< 36D5>
CPU_SHD0_L        5A7<> 5D2<
CPU_SHD1_L        5A7<> 5D2<
CPU_SMI_L         5B3< 5C2< 29C4<>
CPU_SRESET_L      5B2< 5B3< 39D6>
CPU_SRWX_L        5A3< 5C2<
CPU_TA_L          5B3< 8A3<> 8D2< 36D5>
CPU_TBEN          5B3< 5D2< 8A5<>
CPU_TBST_L        5A7> 8B5<> 36D5>
CPU_TEA_L         5B3< 8A3<> 8C2< 36D5>
CPU_THERM_DM_SPN  25A6<
CPU_THERM_DP_SPN  25A6<
CPU_TSIZ<0>       5A7> 8B5<>
CPU_TSIZ<0..2>    36D5>
CPU_TSIZ<1>       5A7> 8B5<>
CPU_TSIZ<2>       5A7> 8B5<>
CPU_TS_L          5C7<> 8D2< 8D5<> 36D5>
CPU_TT<0>         5A7<> 8B5<>
CPU_TT<0..4>      36D5>
CPU_TT<1>         5A7<> 8B5<>
CPU_TT<2>         5A7<> 8B5<>
CPU_TT<3>         5A7<> 8B5<>
CPU_TT<4>         5A7<> 8B5<>
CPU_VCORE_HI_OC   7B8< 29D4<> 33C8< 33D7<
CPU_VCORE_PWR_SEQ  33D8<>
CPU_VCORE_SEQ     33D8<
CPU_VCORE_SEQ_L   33D8<
CPU_VCORE_SLEEP   5D2< 5D8<> 33C1< 33D2< 38D3> 39C6>

CPU_VCORE_SNUB    33B3<
CPU_WT_L          5A7> 8B5<> 36C5>
CSLOT_ADDR3_SPN   13B7>
CSLOT_ADDR4_SPN   13B7>
CSLOT_ADDR5_SPN   13B7>
CSLOT_ADDR6_SPN   13B7>
CSLOT_ADDR7_SPN   13B7>
CSLOT_ADDR8_SPN   13B7>
CSLOT_ADDR9_SPN   13B7>
CSLOT_CE1_L_SPN   13C7>
CSLOT_CE2_L_SPN   13C7>
CSLOT_IORD_L_SPN  13C7>
CSLOT_IOWAIT_L_PU  13C7<
CSLOT_IOWR_L_SPN  13C7>
CSLOT_OE_L_SPN    13C7>
CSLOT_WE_L_SPN    13C7>
CURRENT_THRESHOLD  30C3<
CY25811_S0        19A4<
CY25811_S1        19A4<
DCDC_EN           20A7<> 28C8<> 32B7<> 33C7<>
DCDC_EN_L         32B6< 32B7<> 34C7<>
DDC_CLK_ISO       22D4<>
DDR_VREF          11D1< 11D3<> 11D5<> 11D6<> 11D8<>
                38D3>
DVI_DDC_CLK       22D4<>
DVI_DDC_CLK_UF    22C5<> 22D3<> 39B6>
DVI_DDC_DATA      22C4<>
DVI_DDC_DATA_UF   22C5<> 39B6>
DVI_HPD           22C4<>
DVI_HPD_DIV       22C3<
DVI_HPD_UF        22C3< 22C5<> 39B6>
DVI_TURN_ON       22D3<>
DVI_TURN_ON_BASE  22D2<>
DVI_TURN_ON_ILIM  22D2<
EIDE_ADDR<0>      13B7> 24B8<
EIDE_ADDR<2..0>   37B5>
EIDE_ADDR<1>      13B7> 24B8<
EIDE_ADDR<2>      13B7> 24B8<
EIDE_CS0_L        13B7> 24B8< 37B5>
EIDE_CS1_L        13B7> 24A8< 37B5>
EIDE_DATA<0>      13C7<> 24C8<
EIDE_DATA<15..0>  37B5>
EIDE_DATA<1>      13C7<> 24C8<
EIDE_DATA<2>      13C7<> 24C8<
EIDE_DATA<3>      13C7<> 24C8<
EIDE_DATA<4>      13C7<> 24B8<
EIDE_DATA<5>      13B7<> 24B8<
EIDE_DATA<6>      13B7<> 24B8<
EIDE_DATA<7>      13B7<> 24B8<
EIDE_DATA<8>      13B7<> 24D8<
EIDE_DATA<9>      13B7<> 24C8<
EIDE_DATA<10>     13B7<> 24D8<
EIDE_DATA<11>     13B7<> 24C8<
EIDE_DATA<12>     13B7<> 24C8<
EIDE_DATA<13>     13B7<> 24C8<
EIDE_DATA<14>     13B7<> 24C8<
EIDE_DATA<15>     13B7<> 24C8<
EIDE_DMACK_L      13A7<> 24A8< 37B5>
EIDE_DMARQ        13A7< 24A8< 37B5>
EIDE_INT          13A7< 24A8< 37B5>
EIDE_IOCHRDY      13B7< 24A8< 37B5>
EIDE_OPTICAL_ADDR<0>  24A5<> 24B7<
EIDE_OPTICAL_ADDR<2..0>  37B5> 39C3>
EIDE_OPTICAL_ADDR<1>  24A5<> 24B7<
EIDE_OPTICAL_ADDR<2>  24A6<> 24B7<
EIDE_OPTICAL_CS0_L  24A5<> 24B7< 37B5> 39C3>
EIDE_OPTICAL_CS1_L  24A6<> 24A7< 37B5> 39C3>
EIDE_OPTICAL_DATA<0>  24A5<> 24C7<
EIDE_OPTICAL_DATA<15..0>  37B5> 39C3>
EIDE_OPTICAL_DATA<1>  24A5<> 24C7<
EIDE_OPTICAL_DATA<2>  24A5<> 24C7<
EIDE_OPTICAL_DATA<3>  24A5<> 24C7<
EIDE_OPTICAL_DATA<4>  24A5<> 24B7<
EIDE_OPTICAL_DATA<5>  24A5<> 24B7<
EIDE_OPTICAL_DATA<6>  24A5<> 24B7<
EIDE_OPTICAL_DATA<7>  24A5<> 24B7<
EIDE_OPTICAL_DATA<8>  24A6<> 24D7<
EIDE_OPTICAL_DATA<9>  24A6<> 24C7<
EIDE_OPTICAL_DATA<10>  24A6<> 24D7<
EIDE_OPTICAL_DATA<11>  24A6<> 24C7<
EIDE_OPTICAL_DATA<12>  24A6<> 24C7<
EIDE_OPTICAL_DATA<13>  24A6<> 24C7<
EIDE_OPTICAL_DATA<14>  24A6<> 24C7<
EIDE_OPTICAL_DATA<15>  24A6<> 24C7<
EIDE_OPTICAL_DMAACK_L  24A6<> 24A7< 37A5> 39C3>
EIDE_OPTICAL_DMA_RQ  24A6<> 24A7< 37A5> 39C3>
EIDE_OPTICAL_INT  24A5<> 24A7< 37A5> 39B3>
EIDE_OPTICAL_IOCHRDY  24A5<> 24A7< 37A5> 39B3>
EIDE_OPTICAL_READ_L  24A6<> 24A7< 37B5> 39C3>
EIDE_OPTICAL_RST_L  24A7< 24B5<> 37A5> 39C3>
EIDE_OPTICAL_WR_L  24A5<> 24A7< 37B5> 39B3>
EIDE_RD_L         13A7> 24A8< 37B5>

EIDE_RST_L        13B7> 24A8< 37B5>
EIDE_WR_L         13A7> 24A8< 37B5>
ENET_COL          13C5< 26B7> 37A5>
ENET_COMA         26B7<>
ENET_CRS          13C5< 26B7> 37A5>
ENET_CTAP_CHGND   38A6>
ENET_ENERGY_DET   14B5<> 26B7<>
ENET_HSDACM       26A7<>
ENET_HSDACP       26A7<>
ENET_LINK_RXD<0>  13C5< 26C7>
ENET_LINK_RXD<7..0>  37A5>
ENET_LINK_RXD<1>  13C5< 26C7>
ENET_LINK_RXD<2>  13C5< 26C7>
ENET_LINK_RXD<3>  13C5< 26B7>
ENET_LINK_RXD<4>  13C5< 26B7>
ENET_LINK_RXD<5>  13C5< 26B7>
ENET_LINK_RXD<6>  13C5< 26B7>
ENET_LINK_RXD<7>  13C5< 26B7>
ENET_LINK_TXD<0>  13B4< 13D5>
ENET_LINK_TXD<7..0>  37A5>
ENET_LINK_TXD<1>  13B4< 13D5>
ENET_LINK_TXD<2>  13B4< 13D5>
ENET_LINK_TXD<3>  13B4< 13D5>
ENET_LINK_TXD<4>  13B4< 13D5>
ENET_LINK_TXD<5>  13B4< 13D5>
ENET_LINK_TXD<6>  13A4< 13D5>
ENET_LINK_TXD<7>  13A4< 13D5>
ENET_LINK_TX_EN   13D5<> 37A5>
ENET_LINK_TX_ER   13D5<> 37A5>
ENET_MDC          13C5> 26B7< 37A5>
ENET_MDIO         13C5<> 26B7<> 37A5>
ENET_PHY_TXD<0>   13B5< 26C7<
ENET_PHY_TXD<7..0>  37A5>
ENET_PHY_TXD<1>   13B5< 26C7<
ENET_PHY_TXD<2>   13B5< 26C7<
ENET_PHY_TXD<3>   13B5< 26C7<
ENET_PHY_TXD<4>   13B5< 26C7<
ENET_PHY_TXD<5>   13B5< 26C7<
ENET_PHY_TXD<6>   13A5< 26C7<
ENET_PHY_TXD<7>   13A5< 26C7<
ENET_PHY_TX_EN    13D6< 26C7< 37A5>
ENET_PHY_TX_ER    13D6< 26C7< 37A5>
ENET_RSET         26A5<
ENET_RST_L        26B7<
ENET_RX_DV        13D5< 26B7> 37A5>
ENET_RX_ER        13C5< 26B7> 37A5>
ENET_VSSC         26A7<>
ESP_EN_L          6C2<> 6C2<
FAN1_GND          38B6> 39A3>
FAN1_PWM          25A4<>
FAN1_PWM_L        25A4<> 25B2<>
FAN1_TACH         25A4< 25B2< 39A3>
FAN2_GND          38B6> 39A3>
FAN2_PWM          25A3<>
FAN2_PWM_L        25A3<> 25B2<>
FAN2_TACH         25A3< 25B2< 39A3>
FB_4_85V_BU       31A5<
FP_PWR_EN         20C6<> 22A5< 22B3<>
FP_PWR_EN_L       22B3<>
FWB_TPB0          27A3<
FWB_TPB1          27A3<
FWPLL_BYP         27D8<>
FW_BIAS0          27A4<>
FW_BIAS1          27A4<>
FW_BMODE          27B6<
FW_CORE_ADJ       27C7<
FW_CORE_BYP       27C7<>
FW_CPS            27B6<
FW_GATE_EN        28D6<>
FW_GATE_EN_RC     28C6<>
FW_INPUT_PD       27A6<
FW_LINK_CNTL<0>   13C3<> 27C3<
FW_LINK_CNTL<1..0>  37A5>
FW_LINK_CNTL<1>   13C3<> 27C3<
FW_LINK_DATA<0>   13D3<> 27B7<
FW_LINK_DATA<7..0>  37A5>
FW_LINK_DATA<1>   13D3<> 27B7<
FW_LINK_DATA<2>   13D3<> 27B7<
FW_LINK_DATA<3>   13D3<> 27B7<
FW_LINK_DATA<4>   13C3<> 27B7<
FW_LINK_DATA<5>   13C3<> 27A7<
FW_LINK_DATA<6>   13C3<> 27A7<
FW_LINK_DATA<7>   13C3<> 27A7<
FW_LINK_LREQ      13C3<> 37A5>
FW_LKON           13C3<> 27B4<>
FW_OSC            27A4< 35A1>
FW_OSC_EN         27A3<
FW_PC_PD          27B6<
FW_PC_PU          27B6<
FW_PHY_CNTL<0>    27B4<> 27C4<
FW_PHY_CNTL<1..0>  37A5>
FW_PHY_CNTL<1>    27B4<> 27C4<
FW_PHY_DATA<0>    27B7<>
FW_PHY_DATA<7..0>  37A5>
FW_PHY_DATA<1>    27B7<>
FW_PHY_DATA<2>    27B7<>
FW_PHY_DATA<3>    27B7<>
FW_PHY_DATA<4>    27B7<>
FW_PHY_DATA<5>    27A7<>
FW_PHY_DATA<6>    27A7<>
FW_PHY_DATA<7>    27A7<>
FW_PHY_LPS        13C3<> 27B7<
FW_PHY_LREQ       13C2< 27B7< 37A5>
FW_PHY_PD         14C5<> 27B7<
FW_PHY_RESET_L    27A7<
FW_PINT           13C3<> 27B4> 37A5>
FW_PLL_ADJ        27C7<
FW_PORT1_SEL      27B6<
FW_POWER_UP       28C7<>
FW_R0             27A4<>
FW_R1             27A4<>
FW_TESTM          27A6<
FW_TPA1N          27B2<> 28A4<> 37D2>
FW_TPA1P          27B2<> 28A4<> 37D2>
FW_TPA0N          28C2<> 37D2>
FW_TPA0P          28C2<> 37D2>
FW_TPB1N          27A2<> 28A4<> 37D2>
FW_TPB1P          27B2<> 28A4<> 37D2>
FW_TPB2_PD        27A4<>
FW_TPBI0N         28C2<> 37D2>
FW_TPBI0P         28C2<> 37D2>
FW_TPI0N          27B2<> 28C3<> 37D2> 39A3>
FW_TPI0P          27B2<> 28C3<> 37D2> 39A3>
FW_TPI1N          28A3<> 37D2> 39D1>
FW_TPI1P          28A3<> 37D2> 39D1>
FW_TPO0N          27B2<> 28C3<> 37D2> 39A3>
FW_TPO0P          27B2<> 28C3<> 37D2> 39A3>
FW_TPO0R          28C1<> 39A3>
FW_TPO1N          28A3<> 37D2> 39D1>
FW_TPO1P          28A3<> 37D2> 39D1>
FW_VDD_ON         38A3>
FW_VGND           39A3> 39D1>
FW_VGND0          28C1<> 38A3>
FW_VGND1          28A3<> 38A3>
FW_VREG_PD        27A6<
FW_XI             27A4<> 35A1>
GPU_AGP_TEST      19C6<
GPU_B             20D6<> 22C8<
GPU_B_FILTR       22C8<
GPU_C             20D6<> 22A8<
GPU_COMP          20D6<> 22A8<
GPU_CORE_OK       20A6<> 20D4<> 21D2<> 21D7<>
GPU_DVI_DDC_CLK   20C5<> 22D3<>
GPU_DVI_DDC_DATA  20C5<> 22C3<>
GPU_DVOD<0>       19B3< 19C4<
GPU_DVOD<11..0>   36C1>
GPU_DVOD<1>       19B3< 19C4<
GPU_DVOD<2>       19B3< 19C4<
GPU_DVOD<3>       19B3< 19C4<
GPU_DVOD<4>       19B3< 19C4<
GPU_DVOD<5>       19B3< 19C4<
GPU_DVOD<6>       19B3< 19C4<
GPU_DVOD<7>       19B3< 19C4<
GPU_DVOD<8>       19B2< 19C4<
GPU_DVOD<9>       19B2< 19C4<
GPU_DVOD<10>      19B2< 19C4<
GPU_DVOD<11>      19B2< 19C4<
GPU_DVOD_DE       19B2< 19C4< 36C1>
GPU_DVO_CLKP      19B2< 19C4< 36C1>
GPU_DVO_HSYNC     19B2< 19C4< 36C1>
GPU_DVO_VSYNC     19B2< 19C4< 36C1>
GPU_G             20D6<> 22C8<
GPU_G_FILTR       22C8<
GPU_HPD           20C5< 22C3<>
GPU_MEM_IO        19A6<> 19B8< 21A7< 21B4< 21D2<
                38C3>
GPU_MEM_IO_FLT    21C2< 38C3>
GPU_R             20D6<> 22B8<

GPU_R_FILTR       22B8<
GPU_THERM_DM      19A6<> 25A6<
GPU_THERM_DP      19A6<> 25A6<
GPU_TMDS_CLKN     19B2< 20B8< 20D7< 36D1>
GPU_TMDS_CLKP     19B2< 20B8< 20D8< 36D1>
GPU_TMDS_CLK_CMF  20D7<
GPU_TMDS_D0_CMF   20D7<
GPU_TMDS_D1_CMF   20C7<
GPU_TMDS_D2_CMF   20C7<
GPU_TMDS_DN<0>    19B2< 20B8< 20D7< 36D1>
GPU_TMDS_DN<1>    19B2< 20B8< 20C7< 36D1>
GPU_TMDS_DN<2>    19A2< 20B8< 20C7< 36D1>
GPU_TMDS_DP<0>    19B2< 20B8< 20D8< 36D1>
GPU_TMDS_DP<1>    19B2< 20B8< 20C8< 36D1>
GPU_TMDS_DP<2>    19A2< 20B8< 20C8< 36D1>
GPU_TV_GND1       22B8<> 38B6>
GPU_TV_GND2       22A8<> 38B6>
GPU_VCORE         19D8< 20A3<> 20B5<> 20D4< 38C3>
                39C6>
GPU_VCORE_CNTL    20A3<>
GPU_VCORE_CNTL_L  20A4< 20B7<>
GPU_VCORE_CNTL_RC  20A3<>
GPU_VCORE_NECK    20B5<> 38B3>
GPU_VCORE_PWR_SEQ  20A8<>
GPU_VCORE_SEQ     20A8<
GPU_VCORE_SEQ_L   20A8<
GPU_VCORE_SW      20A4<> 38B1>
GPU_VCORE_VDDCI   19C8< 19D6< 38B3>
GPU_Y             20D6<> 22B8<
HD_ADDR<0>        24C2<> 24C3<
HD_ADDR<2..0>     37C5>
HD_ADDR<1>        24C2<> 24C3<
HD_ADDR<2>        24B3< 24C1<>
HD_CS0_L          24C2<> 24C3< 37B5>
HD_CS1_L          24B3< 24C1<> 37B5>
HD_DATA<0>        24C2<> 24D3<
HD_DATA<15..0>    37C5>
HD_DATA<1>        24C2<> 24D3<
HD_DATA<2>        24D2<> 24D3<
HD_DATA<3>        24D2<> 24D3<
HD_DATA<4>        24C3< 24D2<>
HD_DATA<5>        24C3< 24D2<>
HD_DATA<6>        24C3< 24D2<>
HD_DATA<7>        24C3< 24D2<>
HD_DATA<8>        24C3< 24D1<>
HD_DATA<9>        24C3< 24D1<>
HD_DATA<10>       24C3< 24D1<>
HD_DATA<11>       24D1<> 24D3<
HD_DATA<12>       24B3< 24D1<>
HD_DATA<13>       24B3< 24D1<>
HD_DATA<14>       24C1<> 24C3<
HD_DATA<15>       24B3< 24C1<>
HD_DIOR_L         24A3< 24C2<> 37B5>
HD_DIOW_L         24A3< 24C1<> 37B5>
HD_DMACK_L        24A3< 24C2<> 37B5>
HD_DMARQ          13C6< 24C2<> 37B5>
HD_INTRQ          13C6< 24C1<> 37B5>
HD_IOCHRDY        24A3< 24C1<> 37B5>
HD_RESET_L        24A3< 24D2<> 37C5>
HIGH_VCORE        20A2<>
HIGH_VCORE_DIVD   20A3<
HPD_4V_REF        22C3<
HPD_PWR_SNS_EN    20C7<> 22C3<>
HPD_PWR_SW        22C2<
HPD_PWR_SW_BASE   22C2<>
HPD_REF_EN_L      22C2<>
IAC_FB            30D3<
IAC_RC_COMP       30D3<
ICT_TRST_L        6B2<> 6C2<
INTREPID_ACS_REF  8A5<
INT_AGPPVT        12D4<>
INT_AGP_FB_IN     12C4< 35C1>
INT_AGP_FB_OUT    12C4<> 35C1>
INT_AGP_VREF      12B5< 12D4<> 19D6< 38C3>
INT_CPUFB_IN      8A5< 8B5< 35D1>
INT_CPUFB_IN_NORM  8A4< 35D1>
INT_CPUFB_LONG    8A3< 35D1>
INT_CPUFB_OUT     8A5<> 8A5< 35D1>
INT_CPUFB_OUT_NORM  8A4< 35D1>
INT_CPUFB_OUT_SHORT  8A5< 35D1>
INT_DDRCLK2_N_TP  9B6<>
INT_DDRCLK2_P_TP  9B6<>
INT_DDRCLK5_N_TP  9B6<>
INT_DDRCLK5_P_TP  9B6<>
INT_ENET_RST_L    14B5<> 26B8<
INT_EXTINT3_PU    14A7< 14B5<>
INT_EXTINT8_PU    14B5<> 14C7<
INT_EXTINT10_PU   14B5<> 14B7<
INT_EXTINT11_PU   14B5<> 14B7<
INT_EXTINT12_PU   14B5<> 14B7<
INT_EXTINT13_PU   14B5<> 14B7<
INT_EXTINT14_PU   14B5<> 14C7<
INT_EXTINT16_PU   14B5<> 14B7<
INT_GPIO1_PU      14A7< 14C5<> 33C8<
INT_GPIO9_PU      14A7< 14B5<>
INT_GPIO12_PU     14B5<> 14B7<
INT_GPIO15_PU     14B5<> 14B7<
INT_I2C_CLK0      6B3<> 6D2<> 11A5<> 11A8<> 13C2<
                13C3<> 23D7<> 39C6>
INT_I2C_CLK1      13C2< 13C3<> 14B7< 25B4< 39C6>
INT_I2C_CLK2      14A2<> 25C4<> 25D7<> 39A6>
INT_I2C_DATA0     6B3<> 6D2<> 11A5<> 11A8<> 13C2<
                13C3<> 23D7<> 39C6>
INT_I2C_DATA1     13B2< 13C3<> 14B7< 25B4<> 39C6>
INT_I2C_DATA2     14A2<> 25D4<> 25D7<> 39A6>
INT_I2S0_SND_FROM_ADC  14B2< 25D7<> 39A6>
INT_I2S0_SND_LRCLK  14B1< 25D8<> 39A6>
INT_I2S0_SND_LRCLK_UF  14A3<>
INT_I2S0_SND_MCLK  14B1< 25D8<> 35B1> 39A6>
INT_I2S0_SND_MCLK_UF  14A3<>
INT_I2S0_SND_SCLK  14B1< 25D7<> 39A6>
INT_I2S0_SND_SCLK_UF  14A3<>
INT_I2S0_SND_TO_DAC  14B1< 25D8<> 39A6>
INT_I2S0_SND_TO_DAC_UF  14B3<>
INT_JTAG_TEI      13C2< 13C5< 39D6>
INT_MEM_REF_H     9B6< 38C3>
INT_MEM_VREF      9A7< 9B6<> 38C3>
INT_MOD_BITCLK    14A1< 25D3<>
INT_MOD_BITCLK_UF  14A3<> 14A7<
INT_MOD_CLKOUT    14A1< 25D4<>
INT_MOD_CLKOUT_UF  14A3<> 14A7<
INT_MOD_DTI       14A2< 14A7< 25D3<>
INT_MOD_DTO       14B1< 25D4<>
INT_MOD_DTO_UF    14A3<> 14A7<
INT_MOD_SYNC      14A1< 25D3<>
INT_MOD_SYNC_UF   14A3<> 14A7<
INT_PCI_FB_IN     12C7< 35C1>
INT_PCI_FB_OUT    12C7<> 35C1>
INT_PEND_PROC_INT  14A5> 29C4<>
INT_PROC_SLEEP_REQ_L  14A5< 29B4<>
INT_PU_RESET_L    13D3< 25D5<> 29A2< 29C4<>
INT_REF_CLK_IN    14A5< 14B5< 35C1>
INT_REF_CLK_OUT   14A5< 14B7< 35C1>
INT_REF_CLK_OUT_UF  14A5<> 35C1>
INT_RESET_L       9B3< 13D3< 29C7< 29D4<>
INT_ROM_CS_L      12A5< 12C7>
INT_ROM_OE_L      12A5< 12C7>
INT_ROM_RW_L      12A5< 12C7>
INT_SUSPEND_ACK_L  8B5> 29B6<>
INT_SUSPEND_REQ_L  8B5< 29B6<> 29C7<
INT_TST_MONIN_PD  13C2< 13C5< 39C6>
INT_TST_MONOUT_TP  13C5> 39C6>
INT_TST_PLLEN_PD  13C5< 13D2< 39C6>
INT_WATCHDOG_L    14A5> 29C6<>
INV_GND           22A1<> 39A6>
INV_ON_PWM        20C6<> 22A3<
IO_RESET_L        17A8< 23D7<> 26B8<> 29C6<> 29D7<
JTAG_ASIC_TCK     13C5< 13D2< 26A5< 39D6>
JTAG_ASIC_TDI     13C5< 13D2< 39D6>
JTAG_ASIC_TDO_TP  26A5> 39D6>
JTAG_ASIC_TMS     13C5< 13D2< 26A5< 39D6>
JTAG_ASIC_TRST_L  13C5< 13D2< 26A5< 39D6>
JTAG_CPU_TCK      5B2< 5B3< 6A3> 39D6>
JTAG_CPU_TDI      5B2< 5C3< 6B2<> 39D6>
JTAG_CPU_TDO_TP   5C3> 39D6>
JTAG_CPU_TMS      5B2< 5B3< 6B2<> 39D6>
JTAG_CPU_TRST_L   5A3< 5B3< 6B2<> 39D6>
JTAG_ENET_TDI     13C5> 13D2< 26A5<
KBD_CAPSLOCK_LED  23C1<> 39B3>
KBD_COMMAND_L     23A2< 23C1<> 29C6<> 39B3>
KBD_CONTROL_L     23B2< 23C1<> 29A8< 29C6<> 39A3>
KBD_FUNCTION_L    23A2< 23C1<> 29B6<> 39B3>
KBD_ID            23B2< 23C1<> 29B6<> 39B3>
KBD_INTL          23C1<> 39B3>
KBD_JIS           23C1<> 39B3>
KBD_LED1_OUT      23B5<> 23D7<>
KBD_LED2_OUT      23B4<> 23D7<>
KBD_NUMLOCK_LED   23C1<> 39B3>

KBD_OPTION_L      23A2< 23C1<> 29A8< 29B6<> 39B3>
KBD_SHIFT_L       23A2< 23C1<> 29A8< 29C6<> 39A3>
KBD_X<0>          23B2< 23C1<> 29C6<>
KBD_X<0..9>       39A3>
KBD_X<1>          23B2< 23C1<> 29C6<>
KBD_X<2>          23B2< 23C1<> 29C6<>
KBD_X<3>          23B2< 23C1<> 29C6<>
KBD_X<4>          23B2< 23C1<> 29C6<>
KBD_X<5>          23B2< 23C1<> 29C6<>
KBD_X<6>          23B2< 23D1<> 29C6<>
KBD_X<7>          23B2< 23D1<> 29C6<>
KBD_X<8>          23A2< 23D1<> 29C6<>
KBD_X<9>          23A2< 23D1<> 29C6<>
KBD_Y<0>          23D1<> 29D6<>
KBD_Y<0..7>       39A3>
KBD_Y<1>          23D1<> 29D6<>
KBD_Y<2>          23D1<> 29D6<>
KBD_Y<3>          23D1<> 29D6<>
KBD_Y<4>          23D1<> 29D6<>
KBD_Y<5>          23D1<> 29C6<>
KBD_Y<6>          23D1<> 29C6<>
KBD_Y<7>          23D1<> 29C6<>
LCD_DIGON_L       22B6<
LCD_PWREN_L       22B5<>
LED_LINK10        26B5<>
LED_LINK100       26B5<>
LED_RX_SPN        26B5>
LID_CLOSED_L      23B4<> 39B3>
LM2594_IN         27D8<> 38A3>
LMU_DETECT        23C7< 23D6<> 39D1>
LT1962_INT_ADJ    14D7<
LT1962_INT_BYP    14D7<>
LTC1625_ITH       30D2<>
LTC1962_INT_VIN   14D8<> 38A1>
LTC3405_SW        26D4<> 38A3>
LTC3411_EN_L      34A7<
LTC3411_GND       34A5<> 38A1>
LTC3411_ITH       34A5<> 38A1>
LTC3411_ITH_RC    34A5< 38A1>
LTC3411_SHDN      34A6<> 38A1>
LTC3411_SYNC      34A6<> 38A1>
LTC3411_VCC       34A6< 34A7< 38B1>
LTC3707_START_RC  32B6<
LUX_ALS_GAIN_SW   23B7<> 23D6<>
LUX_ALS_OUT       23B7<> 23D6<>
LVDS_DDC_CLK      20C5<> 22A4< 22B4<> 39B6>
LVDS_DDC_DATA     20C5<> 22A4< 22B4<> 39B6>
LVDS_L0N          20B5> 22B4<> 37C2> 39B6>
LVDS_L0P          20B5> 22B4<> 37C2> 39B6>
LVDS_L1N          20B5> 22B4<> 37C2> 39B6>
LVDS_L1P          20B5> 22B4<> 37C2> 39B6>
LVDS_L2N          20B5> 22A4<> 37C2> 39B6>
LVDS_L2P          20B5> 22A4<> 37C2> 39B6>
LVDS_L3N_TP       20B5>
LVDS_L3P_TP       20B5>
LVDS_U0N          20C5> 22A4<> 37C2>
LVDS_U0P          20C5> 22A4<> 37C2>
LVDS_U1N          20C5> 22A4<> 37C2>
LVDS_U1P          20C5> 22A4<> 37C2>
LVDS_U2N          20B5> 22A4<> 37C2>
LVDS_U2P          20B5> 22A4<> 37C2>
LVDS_U3N_TP       20B5>
LVDS_U3P_TP       20B5>
MAIN_RESET_L      14C7< 17A8< 18A7< 19B8< 19D4<
                24D6<> 29D4<> 29D7< 39C3>
MAX1715_GND       34B5<> 34C5< 38C1>
MAX1715_ON_RC     34C7<>
MAX1715_REF       34B5<> 38C1>
MAX1715_SKIP      34C4< 38C1>
MAX1715_TON       34C5< 38C1>
MAX1715_VCC       34D5< 38C1>
MAX4172_OUT       30D4<>
MAXBUS_SLEEP      5A2< 5D2< 5D5< 6B2< 6B4< 7B7< 7D8<
                8B3< 8B8< 8C8< 8D1< 8D8< 15D8< 16D8<
                33D8< 38D3>
MDI0_PD           26B4<
MDI1_PD           26B4<
MDI2_PD           26B4<
MDI3_PD           26B3<
MDI_M<0>          26B5<> 37D2>
MDI_M<0..3>       39A3>
MDI_M<1>          26B5<> 37D2>
MDI_M<2>          26B5<> 37C2>
MDI_M<3>          26B5<> 37C2>
MDI_P<0>          26B5<> 37D2>
MDI_P<0..3>       39A3>
MDI_P<1>          26B5<> 37D2>
MDI_P<2>          26B5<> 37C2>
MDI_P<3>          26B5<> 37C2>
MEM_ADDR<0>       9B5< 9D6<>
MEM_ADDR<12..0>   35A5>
MEM_ADDR<1>       9B5< 9D6<>
MEM_ADDR<2>       9B5< 9D6<>
MEM_ADDR<3>       9B5< 9D6<>
MEM_ADDR<4>       9B5< 9D6<>
MEM_ADDR<5>       9B5< 9D6<>
MEM_ADDR<6>       9B5< 9D6<>
MEM_ADDR<7>       9B5< 9D6<>
MEM_ADDR<8>       9B5< 9D6<>
MEM_ADDR<9>       9A5< 9D6<>
MEM_ADDR<10>      9A5< 9D6<>
MEM_ADDR<11>      9A5< 9D6<>
MEM_ADDR<12>      9A5< 9D6<>
MEM_BA<0>         9A5< 9D6<>
MEM_BA<1..0>      35A5>
MEM_BA<1>         9A5< 9C6<>
MEM_CAS_L         9A5< 9C6<> 35A5>
MEM_CKE<0>        9B6<> 9C5<
MEM_CKE<3..0>     35A5>
MEM_CKE<1>        9B6<> 9C5<
MEM_CKE<2>        9B6<> 9C5<
MEM_CKE<3>        9B6<> 9C5<
MEM_CS_L<0>       9C5< 9C6<>
MEM_CS_L<3..0>    35A5>
MEM_CS_L<1>       9C5< 9C6<>
MEM_CS_L<2>       9C5< 9C6<>
MEM_CS_L<3>       9C5< 9C6<>
MEM_DATA<0>       9D8<> 10C7<>
MEM_DATA<7..0>    35D5>
MEM_DATA<1>       9D8<> 10C7<>
MEM_DATA<2>       9D8<> 10C7<>
MEM_DATA<3>       9D8<> 10C7<>
MEM_DATA<4>       9D8<> 10C7<>
MEM_DATA<5>       9D8<> 10C7<>
MEM_DATA<6>       9D8<> 10C7<>
MEM_DATA<7>       9D8<> 10C7<>
MEM_DATA<8>       9D8<> 10C7<>
MEM_DATA<15..8>   35D5>
MEM_DATA<9>       9D8<> 10C7<>
MEM_DATA<10>      9D8<> 10C7<>
MEM_DATA<11>      9D8<> 10C7<>
MEM_DATA<12>      9D8<> 10B7<>
MEM_DATA<13>      9C8<> 10B7<>
MEM_DATA<14>      9C8<> 10B7<>
MEM_DATA<15>      9C8<> 10B7<>
MEM_DATA<16>      9C8<> 10C5<>
MEM_DATA<23..16>  35C5>
MEM_DATA<17>      9C8<> 10C5<>
MEM_DATA<18>      9C8<> 10C5<>
MEM_DATA<19>      9C8<> 10C5<>
MEM_DATA<20>      9C8<> 10C5<>
MEM_DATA<21>      9C8<> 10C5<>
MEM_DATA<22>      9C8<> 10C5<>
MEM_DATA<23>      9C8<> 10C5<>
MEM_DATA<24>      9C8<> 10C5<>
MEM_DATA<31..24>  35C5>
MEM_DATA<25>      9C8<> 10C5<>
MEM_DATA<26>      9C8<> 10C5<>
MEM_DATA<27>      9C8<> 10C5<>
MEM_DATA<28>      9C8<> 10C5<>
MEM_DATA<29>      9C8<> 10B5<>
MEM_DATA<30>      9C8<> 10B5<>
MEM_DATA<31>      9C8<> 10B5<>
MEM_DATA<32>      9C8<> 10C3<>
MEM_DATA<39..32>  35C5>
MEM_DATA<33>      9C8<> 10C3<>
MEM_DATA<34>      9C8<> 10C3<>
MEM_DATA<35>      9C8<> 10C3<>
MEM_DATA<36>      9C8<> 10C3<>
MEM_DATA<37>      9C8<> 10C3<>
MEM_DATA<38>      9C8<> 10C3<>
MEM_DATA<39>      9B8<> 10C3<>
MEM_DATA<40>      9B8<> 10C3<>
MEM_DATA<47..40>  35B5>
MEM_DATA<41>      9B8<> 10C3<>
MEM_DATA<42>      9B8<> 10C3<>
MEM_DATA<43>      9B8<> 10C3<>
MEM_DATA<44>      9B8<> 10C3<>

MEM_DATA<45>      9B8<> 10B3<>
MEM_DATA<46>      9B8<> 10B3<>
MEM_DATA<47>      9B8<> 10B3<>
MEM_DATA<48>      9B8<> 10C1<>
MEM_DATA<55..48>  35B5>
MEM_DATA<49>      9B8<> 10C1<>
MEM_DATA<50>      9B8<> 10C1<>
MEM_DATA<51>      9B8<> 10C1<>
MEM_DATA<52>      9B8<> 10C1<>
MEM_DATA<53>      9B8<> 10C1<>
MEM_DATA<54>      9B8<> 10C1<>
MEM_DATA<55>      9B8<> 10C1<>
MEM_DATA<56>      9B8<> 10C1<>
MEM_DATA<63..56>  35A5>
MEM_DATA<57>      9B8<> 10C1<>
MEM_DATA<58>      9B8<> 10C1<>
MEM_DATA<59>      9B8<> 10C1<>
MEM_DATA<60>      9B8<> 10C1<>
MEM_DATA<61>      9B8<> 10B1<>
MEM_DATA<62>      9B8<> 10B1<>
MEM_DATA<63>      9B8<> 10B1<>
MEM_DQM<0>        9C6<> 10C7<> 35D5>
MEM_DQM<1>        9C6<> 10B7<> 35D5>
MEM_DQM<2>        9C6<> 10C5<> 35C5>
MEM_DQM<3>        9C6<> 10B5<> 35C5>
MEM_DQM<4>        9C6<> 10C3<> 35B5>
MEM_DQM<5>        9C6<> 10B3<> 35B5>
MEM_DQM<6>        9C6<> 10C1<> 35B5>
MEM_DQM<7>        9C6<> 10B1<> 35A5>
MEM_DQS<0>        9C6<> 10C7<> 35D5>
MEM_DQS<1>        9C6<> 10B7<> 35D5>
MEM_DQS<2>        9C6<> 10C5<> 35C5>
MEM_DQS<3>        9C6<> 10B5<> 35C5>
MEM_DQS<4>        9C6<> 10C3<> 35B5>
MEM_DQS<5>        9C6<> 10B3<> 35B5>
MEM_DQS<6>        9C6<> 10C1<> 35B5>
MEM_DQS<7>        9C6<> 10B1<> 35A5>
MEM_MUXSEL_LSB    9B6<> 10B5<> 10B7<> 35A5>
MEM_MUXSEL_LSB_L_TP  9B6<>
MEM_MUXSEL_MSB    9B6<> 10B1<> 10B3<> 35A5>
MEM_MUXSEL_MSB_L_TP  9B6<>
MEM_RAS_L         9A5< 9C6<> 35A5>
MEM_WE_L          9A5< 9C6<> 35A5>
MODEM_USB_DM      14B1< 25D3<> 37B2> 39D3>
MODEM_USB_DP      14C1< 25D3<> 37B2> 39D3>
MPIC_CPU_INT_L    5B2< 5B3< 14B5>
NEC_AMC_TP        17A5<
NEC_AVDD          17D5< 38A3>
NEC_AVSS_F        17A5< 17B4<
NEC_CRUN_L        17A7<>
NEC_IDSEL         17B7<
NEC_IO_RESET_L    17A7< 17B7<
NEC_LEGC          17A7< 17A8<
NEC_LUSB_OCI      17B3< 17B5<
NEC_LUSB_OCI_UF   17B1< 25D8<> 39A6>
NEC_LUSB_PPON     17B5> 25D8<> 39A6>
NEC_MAIN_RESET_L  17A7< 17A7<
NEC_NANDTESTEN_TP  17A4<
NEC_NANDTESTOUT_TP  17A4<>
NEC_NC<1>         17B5<>
NEC_NC<2>         17B5<>
NEC_OCI<3>        17B5<
NEC_OCI<4>        17B5<
NEC_OCI<5>        17B5<
NEC_PCI_GNT_L     12C7<> 17B7<
NEC_PCI_INTA_L    17B7<>
NEC_PCI_INTB_L    17B7<>
NEC_PCI_INTC_L    17B7<>
NEC_PCI_INT_L     14B5<> 14D7< 17B8<
NEC_PCI_REQ_L     12A7< 12D7<> 17B7>
NEC_PME_L         17A7> 17A7<
NEC_PPON3_TP      17B5>
NEC_PPON4_TP      17B5>
NEC_PPON5_TP      17B5>
NEC_RREF          17B5<>
NEC_RUSB_OCI      17B3< 17B5<
NEC_RUSB_OCI_UF   17B1< 25D1<> 39D3>
NEC_RUSB_PPON     17B5> 25D1<> 39D3>
NEC_SMI_L_TP      17A7>
NEC_USB_DAM       17D2<> 25D7<> 37B2> 39D3>
NEC_USB_DAP       17D2<> 25D7<> 37B2> 39D3>
NEC_USB_DBM       17C2<> 25D2<> 37B2> 39D3>
NEC_USB_DBP       17C2<> 25D2<> 37A2> 39D3>
NEC_USB_RSDM1     17C5<>
NEC_USB_RSDM2     17C5<>
NEC_USB_RSDP1     17C5<>
NEC_USB_RSDP2     17C5<>
NEC_XT1           17D5<
NEC_XT2           17D5<>
NEC_XT2_R         17D4<
NUMLOCK_LED       23D2<
NUMLOCK_LED_L     23D2< 29C7<
OVER_18V_ADJ      30C3<>
PCI1510_VR_EN_L   18C7<
PCI_AD<0>         9C3< 12D6<> 17D7<> 18C7<> 24B5<>
PCI_AD<31..0>     37C5> 39D3>
PCI_AD<1>         9C3< 12D6<> 17D7<> 18C7<> 24B6<>
PCI_AD<2>         9C3< 12D6<> 17D7<> 18C7<> 24C5<>
PCI_AD<3>         9C3< 12D6<> 17C7<> 18C7<> 24C6<>
PCI_AD<4>         9C3< 12D6<> 17C7<> 18C7<> 24C5<>
PCI_AD<5>         9C3< 12D6<> 17C7<> 18C7<> 24C6<>
PCI_AD<6>         9C3< 12C6<> 17C7<> 18C7<> 24C5<>
PCI_AD<7>         9C3< 12C6<> 17C7<> 18C7<> 24C6<>
PCI_AD<8>         9C3< 12C6<> 17C7<> 18C7<> 24C6<>
PCI_AD<9>         9C3< 12C6<> 17C7<> 18C7<> 24C5<>
PCI_AD<10>        9C3< 12C6<> 17C7<> 18C7<> 24C6<>
PCI_AD<11>        9C3< 12C6<> 17C7<> 18C7<> 24C5<>
PCI_AD<12>        9C3< 12C6<> 17C7<> 18C7<> 24C6<>
PCI_AD<13>        9C3< 12C6<> 17C7<> 18C7<> 24C5<>
PCI_AD<14>        9C3< 12C6<> 17C7<> 18C7<> 24C6<>
PCI_AD<15>        9C3< 12C6<> 17C7<> 18C7<> 24C5<>
PCI_AD<16>        9C3< 12C6<> 17C7<> 18C7<> 24C5<>
PCI_AD<17>        9C3< 12C6<> 17C7<> 18C7<> 24C6<>
PCI_AD<18>        9C3< 12C6<> 17C7<> 18B7<> 24C5<>
                24D4<
PCI_AD<19>        9B3< 12C6<> 17C7<> 18B7<> 24C6<>
PCI_AD<20>        9B3< 12C6<> 17C7<> 18B7<> 24C5<>
PCI_AD<21>        12C6<> 17C7<> 18B7<> 24C6<>
PCI_AD<22>        12C6<> 17C7<> 18B7<> 24C5<>
PCI_AD<23>        12C6<> 17C7<> 18B7<> 24C6<>
PCI_AD<24>        9C1<> 12C6<> 17C7<> 18B7<> 24C5<>
PCI_AD<25>        9C1<> 12C6<> 17C7<> 18B7<> 24C6<>
PCI_AD<26>        9C1<> 12C6<> 17C7<> 18B7<> 24C5<>
PCI_AD<27>        9C1<> 12C6<> 17C8<> 18B7<> 24D6<>
PCI_AD<28>        9C1<> 12C6<> 17C7<> 18B7<> 24C5<>
PCI_AD<29>        9C1<> 12C6<> 17B7<> 18B7<> 24D6<>
PCI_AD<30>        9C1<> 12C6<> 17B7<> 18B7<> 24D5<>
PCI_AD<31>        9C1<> 12C6<> 17B7<> 18B7<> 24D6<>
PCI_CBE<0>        12C7<> 17B7<> 18B7<> 24C5<>
PCI_CBE<3..0>     37C5>
PCI_CBE<1>        12C7<> 17B7<> 18B7<> 24C6<>
PCI_CBE<2>        12C7<> 17B7<> 18B7<> 24C6<>
PCI_CBE<3>        12C7<> 17B7<> 18B7<> 24C6<>
PCI_DEVSEL_L      12B7< 12C7<> 17B7<> 18A7<> 24C5<>
                37C5> 39C3>
PCI_FRAME_L       12B7< 12C7<> 17B7<> 18B7<> 24C5<>
                37C5> 39D3>
PCI_IRDY_L        12B7< 12C7<> 17B7<> 18B7<> 24C6<>
                37C5> 39D3>
PCI_PAR           12C7<> 17B7<> 18B7<> 24C5<> 37C5>
                39C3>
PCI_PERR_L        17B7<> 18B7<> 18D7<
PCI_SERR_L        17B7> 18B7> 18D7<
PCI_STOP_L        12A7< 12C7<> 17B7<> 18B7<> 24C5<>
                37C5> 39C3>
PCI_TRDY_L        12B7< 12C7<> 17B7<> 18A7<> 24C5<>
                37C5> 39D3>
PLL_STOP_L        7C4<> 7C8<>
PMU_ACK_L         14C2< 29C4<>
PMU_AC_DET        29A4< 29B4<>
PMU_AC_IN         29B4<>
PMU_BATT0_DET_L   29B4<>
PMU_BATT1_DET_L_PU  29B4<> 29D2<
PMU_BATT_DET_L    29B3< 29D2< 30A4<> 39A3>
PMU_BYTE          29B6< 29C7<
PMU_CAPSLOCK_LED_L  29C6<>
PMU_CHARGE_V      29C4<> 30B8<>
PMU_CHRG_BATT_0   29C4<> 30A8<>
PMU_CLK           14C2<> 29C4<>
PMU_CNVSS         29B6< 29C7<
PMU_CPU_HRESET_L  6A2< 6C3<> 29C4<> 39C1>
PMU_EPM           29C4<> 29D2<
PMU_FROM_INT      14C2<> 29C4<>
PMU_I2C_CLK       29B4<> 29C2<
PMU_I2C_DATA      29B4<> 29C2<
PMU_INT_L         14B5<> 14B7< 29B6<>
PMU_INT_NMI       14B5<> 14B7< 29D4<>
PMU_KB_RESET_IN1  29A7<>
```

```
PMU_KB_RESET_IN2  29A7<>
PMU_KB_RESET_L    29A6> 29B7< 39C1>
PMU_LID_CLOSED_L  23B3< 23D6<> 29B2< 29C4<> 39D1>
PMU_NMI_BUTTON_L  29C2< 29C4<>
PMU_NMI_L         29C2< 29C4<>
PMU_NUMLOCK_LED_L 29C6<>
PMU_OOPS          29B2< 29B4<>
PMU_PME_L         14A5<> 17A8< 24D5<> 29B2< 29C4<>
                  39C3>
PMU_POWERUP_OK    29B4<> 29D2<
PMU_POWER_UP_L    28C8<> 29C6<> 29D7< 32B8<
PMU_REQ_L         14B7< 14C2> 29C4<>
PMU_RESET_BUTTON_L  23A7< 29C4<> 29D2<
PMU_RESET_L       29B6<>
PMU_SLEEP_LED     23C7<> 23D6<> 39D1>
PMU_SLEEP_LED_L   23C8<> 29C4<>
PMU_SMB_CLK       29B4<> 29C2< 30A3<
PMU_SMB_DATA      29B4<> 29C2< 30A2<
PMU_TO_INT        14C2<> 29C4<>
POWER_UP          28D7<>
POWER_VALID       29B2< 29C4<>
PWR_BUTTON_L      23A7< 23B4<>
RAM_ADDR<0>       9B4< 11B3<> 11B6<>
RAM_ADDR<12..0>   35A5>
RAM_ADDR<1>       9B4< 11B5<> 11B8<>
RAM_ADDR<2>       9B4< 11B3<> 11B6<>
RAM_ADDR<3>       9B4< 11B5<> 11B8<>
RAM_ADDR<4>       9B4< 11B3<> 11B6<>
RAM_ADDR<5>       9B4< 11B5<> 11B8<>
RAM_ADDR<6>       9B4< 11B3<> 11B6<>
RAM_ADDR<7>       9B4< 11B5<> 11B8<>
RAM_ADDR<8>       9B4< 11B3<> 11B6<>
RAM_ADDR<9>       9A4< 11B5<> 11B8<>
RAM_ADDR<10>      9A4< 11B5<> 11B8<>
RAM_ADDR<11>      9A4< 11B3<> 11B6<>
RAM_ADDR<12>      9A4< 11B5<> 11B8<>
RAM_BA<0>         9A4< 11B5<> 11B8<>
RAM_BA<1..0>      35A5>
RAM_BA<1>         9A4< 11B3<> 11B6<>
RAM_CAS_L         9A4< 11B3<> 11B6<> 35A5>
RAM_CKE<0>        9A4< 9C4< 11C6<>
RAM_CKE<3..0>     35A5<
RAM_CKE<1>        9A4< 9C4< 11C8<>
RAM_CKE<2>        9A4< 9C4< 11C3<>
RAM_CKE<3>        9A4< 9C4< 11C5<>
RAM_CS_L<0>       9C4< 11B8<>
RAM_CS_L<3..0>    35A5>
RAM_CS_L<1>       9C4< 11B6<>
RAM_CS_L<2>       9C4< 11B5<>
RAM_CS_L<3>       9C4< 11B3<>
RAM_DATA_A<0>     10C8<> 11D8<>
RAM_DATA_A<7..0>  35D5>
RAM_DATA_A<1>     10C8<> 11D6<>
RAM_DATA_A<2>     10C8<> 11D8<>
RAM_DATA_A<3>     10B8<> 11D8<>
RAM_DATA_A<4>     10B8<> 11D6<>
RAM_DATA_A<5>     10B8<> 11D6<>
RAM_DATA_A<6>     10B8<> 11D6<>
RAM_DATA_A<7>     10B8<> 11D6<>
RAM_DATA_A<8>     10B8<> 11D8<>
RAM_DATA_A<15..8> 35C5>
RAM_DATA_A<9>     10C7<> 11D8<>
RAM_DATA_A<10>    10C7<> 11D8<>
RAM_DATA_A<11>    10C7<> 11D8<>
RAM_DATA_A<12>    10C7<> 11D6<>
RAM_DATA_A<13>    10C7<> 11D6<>
RAM_DATA_A<14>    10C7<> 11D6<>
RAM_DATA_A<15>    10C7<> 11D6<>
RAM_DATA_A<16>    10C6<> 11D8<>
RAM_DATA_A<23..16>  35C5>
RAM_DATA_A<17>    10C6<> 11C8<>
RAM_DATA_A<18>    10C6<> 11C8<>
RAM_DATA_A<19>    10B6<> 11C8<>
RAM_DATA_A<20>    10B6<> 11D6<>
RAM_DATA_A<21>    10B6<> 11C6<>
RAM_DATA_A<22>    10B6<> 11C6<>
RAM_DATA_A<23>    10B6<> 11C6<>
RAM_DATA_A<24>    10B6<> 11C8<>
RAM_DATA_A<31..24>  35C5>
RAM_DATA_A<25>    10C5<> 11C8<>
RAM_DATA_A<26>    10C5<> 11C8<>
RAM_DATA_A<27>    10C5<> 11C8<>
RAM_DATA_A<28>    10C5<> 11C6<>
RAM_DATA_A<29>    10C5<> 11C6<>
RAM_DATA_A<30>    10C5<> 11C6<>
RAM_DATA_A<31>    10C5<> 11C6<>
RAM_DATA_A<32>    10C4<> 11B8<>
RAM_DATA_A<39..32>  35B5>
RAM_DATA_A<33>    10C4<> 11B8<>
RAM_DATA_A<34>    10C4<> 11B8<>
RAM_DATA_A<35>    10C4<> 11B8<>
RAM_DATA_A<36>    10B4<> 11B6<>
RAM_DATA_A<37>    10B4<> 11B6<>
RAM_DATA_A<38>    10B4<> 11B6<>
RAM_DATA_A<39>    10B4<> 11B6<>
RAM_DATA_A<40>    10B4<> 11B8<>
RAM_DATA_A<47..40>  35B5>
RAM_DATA_A<41>    10D3<> 11B8<>
RAM_DATA_A<42>    10C3<> 11A8<>
RAM_DATA_A<43>    10C3<> 11A8<>
RAM_DATA_A<44>    10C3<> 11B6<>
RAM_DATA_A<45>    10C3<> 11B6<>
RAM_DATA_A<46>    10C3<> 11A6<>
RAM_DATA_A<47>    10C3<> 11A6<>
RAM_DATA_A<48>    10C2<> 11A8<>
RAM_DATA_A<55..48>  35B5>
RAM_DATA_A<49>    10C2<> 11A8<>
RAM_DATA_A<50>    10C2<> 11A8<>
RAM_DATA_A<51>    10C2<> 11A8<>
RAM_DATA_A<52>    10B2<> 11A6<>
RAM_DATA_A<53>    10B2<> 11A6<>
RAM_DATA_A<54>    10B2<> 11A6<>
RAM_DATA_A<55>    10B2<> 11A6<>
RAM_DATA_A<56>    10B2<> 11A8<>
RAM_DATA_A<63..56>  35A5>
RAM_DATA_A<57>    10D1<> 11A8<>
RAM_DATA_A<58>    10C1<> 11A8<>
RAM_DATA_A<59>    10C1<> 11A8<>
RAM_DATA_A<60>    10C1<> 11A6<>
RAM_DATA_A<61>    10C1<> 11A6<>
RAM_DATA_A<62>    10C1<> 11A6<>
RAM_DATA_A<63>    10C1<> 11A6<>
RAM_DATA_B<0>     10C8<> 11D5<>
RAM_DATA_B<7..0>  35D5>
RAM_DATA_B<1>     10C8<> 11D5<>
RAM_DATA_B<2>     10C8<> 11D5<>
RAM_DATA_B<3>     10B8<> 11D5<>
RAM_DATA_B<4>     10C8<> 11D3<>
RAM_DATA_B<5>     10C8<> 11D3<>
RAM_DATA_B<6>     10C8<> 11D3<>
RAM_DATA_B<7>     10C8<> 11D3<>
RAM_DATA_B<8>     10C8<> 11D5<>
RAM_DATA_B<15..8> 35C5>
RAM_DATA_B<9>     10C8<> 11D5<>
RAM_DATA_B<10>    10C8<> 11D5<>
RAM_DATA_B<11>    10C8<> 11D5<>
RAM_DATA_B<12>    10C8<> 11D3<>
RAM_DATA_B<13>    10C8<> 11D3<>
RAM_DATA_B<14>    10C8<> 11D3<>
RAM_DATA_B<15>    10C8<> 11D3<>
RAM_DATA_B<16>    10C6<> 11D5<>
RAM_DATA_B<23..16>  35C5>
RAM_DATA_B<17>    10C6<> 11C5<>
RAM_DATA_B<18>    10C6<> 11C5<>
RAM_DATA_B<19>    10C6<> 11C5<>
RAM_DATA_B<20>    10C6<> 11D3<>
RAM_DATA_B<21>    10C6<> 11C3<>
RAM_DATA_B<22>    10C6<> 11C3<>
RAM_DATA_B<23>    10C6<> 11C3<>
RAM_DATA_B<24>    10C6<> 11C5<>
RAM_DATA_B<25..24>  35C5>
RAM_DATA_B<25>    10C6<> 11C5<>
RAM_DATA_B<26>    10C6<> 11C5<> 35C5>
RAM_DATA_B<27>    10C6<> 11C5<>
RAM_DATA_B<31..27>  35C5>
RAM_DATA_B<28>    10C6<> 11C3<>
RAM_DATA_B<29>    10C6<> 11C3<>
RAM_DATA_B<30>    10C6<> 11C3<>
RAM_DATA_B<31>    10C6<> 11C3<>
RAM_DATA_B<32>    10D4<> 11B5<>
RAM_DATA_B<39..32>  35B5>
RAM_DATA_B<33>    10C4<> 11B5<>
RAM_DATA_B<34>    10C4<> 11B5<>
RAM_DATA_B<35>    10C4<> 11B5<>
RAM_DATA_B<36>    10C4<> 11B3<>
RAM_DATA_B<37>    10C4<> 11B3<>
RAM_DATA_B<38>    10C4<> 11B3<>
RAM_DATA_B<39>    10C4<> 11B3<>
```

```
RAM_DATA_B<40>    10C4<> 11B5<>
RAM_DATA_B<47..40>  35B5>
RAM_DATA_B<41>    10C4<> 11B5<>
RAM_DATA_B<42>    10C4<> 11A5<>
RAM_DATA_B<43>    10C4<> 11A5<>
RAM_DATA_B<44>    10C4<> 11B3<>
RAM_DATA_B<45>    10C4<> 11B3<>
RAM_DATA_B<46>    10C4<> 11A3<>
RAM_DATA_B<47>    10C4<> 11A3<>
RAM_DATA_B<48>    10D2<> 11A5<>
RAM_DATA_B<55..48>  35B5>
RAM_DATA_B<49>    10C2<> 11A5<>
RAM_DATA_B<50>    10C2<> 11A5<>
RAM_DATA_B<51>    10C2<> 11A5<>
RAM_DATA_B<52>    10C2<> 11A3<>
RAM_DATA_B<53>    10C2<> 11A3<>
RAM_DATA_B<54>    10C2<> 11A3<>
RAM_DATA_B<55>    10C2<> 11A3<>
RAM_DATA_B<56>    10C2<> 11A5<>
RAM_DATA_B<63..56>  35A5>
RAM_DATA_B<57>    10C2<> 11A5<>
RAM_DATA_B<58>    10C2<> 11A5<>
RAM_DATA_B<59>    10C2<> 11A5<>
RAM_DATA_B<60>    10C2<> 11A3<>
RAM_DATA_B<61>    10C2<> 11A3<>
RAM_DATA_B<62>    10C2<> 11A3<>
RAM_DATA_B<63>    10C2<> 11A3<>
RAM_DQM_A<0>      10B8<> 11D6<> 35D5>
RAM_DQM_A<1>      10C7<> 11D6<> 35C5>
RAM_DQM_A<2>      10B6<> 11C6<> 35C5>
RAM_DQM_A<3>      10C5<> 11C6<> 35C5>
RAM_DQM_A<4>      10B4<> 11B6<> 35B5>
RAM_DQM_A<5>      10C3<> 11B6<> 35B5>
RAM_DQM_A<6>      10B2<> 11A6<> 35B5>
RAM_DQM_A<7>      10C1<> 11A6<> 35A5>
RAM_DQM_B<0>      10C8<> 11D3<> 35D5>
RAM_DQM_B<1>      10C8<> 11D3<> 35C5>
RAM_DQM_B<2>      10C6<> 11C3<> 35C5>
RAM_DQM_B<3>      10C6<> 11C3<> 35C5>
RAM_DQM_B<4>      10C4<> 11B3<> 35B5>
RAM_DQM_B<5>      10C4<> 11B3<> 35B5>
RAM_DQM_B<6>      10C2<> 11A3<> 35B5>
RAM_DQM_B<7>      10C2<> 11A3<> 35A5>
RAM_DQS_A<0>      10B8<> 11D8<> 35D5>
RAM_DQS_A<1>      10C7<> 11D8<> 35C5>
RAM_DQS_A<2>      10B6<> 11C8<> 35C5>
RAM_DQS_A<3>      10C5<> 11C8<> 35C5>
RAM_DQS_A<4>      10B4<> 11B8<> 35B5>
RAM_DQS_A<5>      10C3<> 11B8<> 35B5>
RAM_DQS_A<6>      10B2<> 11A8<> 35B5>
RAM_DQS_A<7>      10C1<> 11A8<> 35A5>
RAM_DQS_B<0>      10C8<> 11D5<> 35D5>
RAM_DQS_B<1>      10C8<> 11D5<> 35C5>
RAM_DQS_B<2>      10C6<> 11C5<> 35C5>
RAM_DQS_B<3>      10C6<> 11C5<> 35C5>
RAM_DQS_B<4>      10C4<> 11B5<> 35B5>
RAM_DQS_B<5>      10C4<> 11B5<> 35B5>
RAM_DQS_B<6>      10C2<> 11A5<> 35B5>
RAM_DQS_B<7>      10C2<> 11A5<> 35A5>
RAM_RAS_L         9A4< 11B3<> 11B6<> 35A5>
RAM_WE_L          9A4< 11B5<> 11B8<> 35A5>
RESET_VREF        6C3<>
RF_DISABLE_L      24D6<> 39C3>
ROM_CS_L          9B3< 12A4< 24B6<> 39C3>
ROM_OE_L          9B3< 12A4< 24C5<> 39C3>
ROM_ONBOARD_CS_L  9B3< 24C6<> 39C3>
ROM_RW_L          9B3< 12A4< 24C6<> 39C3>
ROM_WP_L          9B3<
SI_A2             19C4<
SI_EXT_SWING_SET  19C2<>
SI_HPD            19C4<
SI_I2C_CLK        19D4< 20C5<>
SI_I2S_DATA       19C4< 20C5<>
SI_MSEN           19D2<>
SI_PD_L           19C4<
SI_RST_L          19C4<
SI_TMDS_CLKN      19C2< 19C2<> 36D1>
SI_TMDS_CLKP      19C2<> 19C2< 36D1>
SI_TMDS_CLK_STM   19D1<
SI_TMDS_D0_STM    19D1<
SI_TMDS_D1_STM    19D1<
SI_TMDS_D2_STM    19C1<
SI_TMDS_DN<0>     19C2< 19C2<> 36D1>
SI_TMDS_DN<1>     19B2< 19C2<> 36D1>
SI_TMDS_DN<2>     19B2< 19C2<> 36C1>
SI_TMDS_DP<0>     19C2< 19C2<> 36C1>
SI_TMDS_DP<1>     19B2< 19C2<> 36C1>
SI_TMDS_DP<2>     19B2< 19C2<> 36C1>
SI_VREF_IDCK_N    19C2< 19C4<
SLEEP             23D7<> 25D7<> 29B6<> 29D7< 32A4<
                  32A6< 32B3< 32B8<> 34B3< 34C2< 39C1>
SLEEP_LED         23C3<> 39C1>
SLEEP_LED_DGND    23C3<>
SLEEP_LED_I       23D3<
SLEEP_LED_L       23D4<
SLEEP_LED_SW_L    23D4<>
SLEEP_LED_UF      23D3<
SLEEP_LS5         32A4<> 32A8<
SLEEP_LS5_EN_L    32A5<>
SLEEP_L_LS5       18D5< 20A7<> 26A8<> 32A5<> 33C7<>
                  34C8<
SLEEP_L_LS5_EN_L  32A6<>
SLEEP_L_LS5_INV   34A3< 34C2< 34C8<>
SLEEP_L_LS5_NET   32B3<> 34C8<>
SLEEP_NET         32A3<>
SLEEP_NET_INV     32A3<>
SND_AMP_MUTE      25C7<> 25D6<> 39A6>
SND_AMP_MUTE_CTRL 25B5<> 25D6<>
SND_AMP_MUTE_L    14B5<> 25D5<>
SND_HP_MUTE       25C5<>
SND_HP_MUTE_L     14C5<> 25C5<> 39A6>
SND_HP_MUTE_LO    25C6<> 25C7<>
SND_HP_SENSE_L    14B5<> 25C8<> 39A6>
SND_HW_RESET_L    14A7< 14B5<> 25D7<> 39A6>
SND_LIN_SENSE_L   14B5<> 25C8<> 39A6>
SOFT_PWR_ON_L     22D1<> 23A3< 29A8< 29C6<> 29D7<
                  33A4<> 39B3>
ST7_SLEEP_LED_H   23C5<> 23C6<> 23D6<> 39D1>
STOP_AGP_L        12D2< 12D4<>
SYSCLK_CPU        5C3< 8A6< 35D1>
SYSCLK_CPU_UF     8A5<> 35D1>
SYSCLK_DDRCLK_A0  9D4< 11D8<> 35D1>
SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 35C1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_A1  9D4< 11A6<> 35C1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 35C1>
SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_B0  9D4< 11D5<> 35C1>
SYSCLK_DDRCLK_B0_L  9C4< 11D5<> 35C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 35D1>
SYSCLK_DDRCLK_B0_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_B1  9D4< 11A3<> 35C1>
SYSCLK_DDRCLK_B1_L  9D4< 11A3<> 35C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_B1_UF  9B6<> 9D5< 35D1>
SYSCLK_LA_TP      8A5<>
SYSTEM_CLK_EN     14A5< 14B7< 29C4<>
THERM1_A_DM       25A7< 25A8< 37A2>
THERM1_A_DP       25A7< 25A8< 37A2>
THERM1_DM         25A5< 25A6< 25B5<> 25B6< 37A2>
THERM1_DP         25A5< 25A6< 25B5<> 25B6< 37A2>
THERM1_M_DM       25B7< 25B8< 37A2>
THERM1_M_DP       25B7< 25B8< 37A2>
THERM2_A_DM       25A7< 25A8< 37A2>
THERM2_A_DP       25A7< 25A8< 37A2>
THERM2_DM         25A5< 25A6< 25B5<> 25B6< 37A2>
THERM2_DP         25A5< 25A6< 25B5<> 25B6< 37A2>
THERM2_M_DM       25B7< 25B8< 37A2>
THERM2_M_DP       25B7< 25B8< 37A2>
THERM_INV         25B1<>
THERM_L_OC        25B1<> 29B4<>
TMDS_CLKN         19B1< 19C1< 19D1< 22C8<> 37C2>
TMDS_CLKP         19B1< 19C1< 19D2< 22C8<> 37C2>
TMDS_CONN_CLKN    22C7<> 22C7<> 36C1> 39C6>
TMDS_CONN_CLKP    22C7<> 22C7<> 36C1> 39C6>
TMDS_CONN_DN<0>   22D6<> 36C1>
TMDS_CONN_DN<1>   22D6<> 36B1>
TMDS_CONN_DN<2>   22D6<> 36B1>
TMDS_CONN_DP<0>   22D6<> 36C1>
TMDS_CONN_DP<1>   22D6<> 36B1>
TMDS_CONN_DP<2>   22D6<> 36B1>
TMDS_DN<0>        19B1< 19C1< 19D1< 22D7<> 37C2>
TMDS_DN<0..2>     39C6>
TMDS_DN<1>        19B1< 19B1< 19C1< 22D5<> 37B2>
TMDS_DN<2>        19A1< 19B1< 19C1< 22D5<> 37B2>
```

```
TMDS_DP<0>        19B1< 19C1< 19D2< 22D7<> 37B2>
TMDS_DP<0..2>     39C6>
TMDS_DP<1>        19B1< 19B1< 19C2< 22C5<> 37B2>
TMDS_DP<2>        19A1< 19B1< 19C2< 22D5<> 37B2>
TPAD_F_RXD        23B5<> 39B3>
TPAD_F_TXD        23B5<> 39B3>
TPAD_RXD          23A5< 29C2< 29C4<>
TPAD_TXD          23B5< 29B2< 29C4<>
TPS2211_SHTDWN_L  18C5<
TV_C              22A6<> 39A6>
TV_COMP           22A6<> 39A6>
TV_GND1           22B6<> 38B6> 39A6>
TV_GND2           22A6<> 38B6> 39A6>
TV_Y              22A6<> 39A6>
UIDE_ADDR<0>      13D7> 24C4<
UIDE_ADDR<2..0>   37C5>
UIDE_ADDR<1>      13D7> 24C4<
UIDE_ADDR<2>      13D7> 24B4<
UIDE_CS0_L        13C7> 24C4< 37C5>
UIDE_CS1_L        13C7> 24B4< 37C5>
UIDE_DATA<8>      13D7> 24D4<
UIDE_DATA<6..0>   37C5>
UIDE_DATA<1>      13D7> 24D4<
UIDE_DATA<2>      13D7> 24D4<
UIDE_DATA<3>      13D7> 24D4<
UIDE_DATA<4>      13D7> 24C4<
UIDE_DATA<5>      13D7> 24C4<
UIDE_DATA<6>      13D7> 24C4<
UIDE_DATA<7>      13D7> 24C4< 37C5>
UIDE_DATA<8>      13D7> 24C4<
UIDE_DATA<15..8>  37C5>
UIDE_DATA<9>      13D7> 24C4<
UIDE_DATA<10>     13D7> 24C4<
UIDE_DATA<11>     13D7> 24D4<
UIDE_DATA<12>     13D7> 24B4<
UIDE_DATA<13>     13D7> 24B4<
UIDE_DATA<14>     13D7> 24C4<
UIDE_DATA<15>     13D7> 24B4<
UIDE_DIOR_L       13C7> 24A4< 37C5>
UIDE_DIOW_L       13C7> 24A4< 37C5>
UIDE_DMACK_L      13C7> 24A4< 37C5>
UIDE_DMARQ        13C7> 37C5>
UIDE_INTRQ        13C7< 37C5>
UIDE_IOCHRDY      13C7< 24A4< 37C5>
UIDE_REF          13C7<> 38C3>
UIDE_RST_L        13C7> 24A4< 37C5>
USB_DAM           14B2<> 14D2<
USB_DAP           14B2<> 14D2<
USB_DBM           14B2<> 14D2<
USB_DBP           14B2<> 14D2<
USB_DCM           14B2<> 14D2<
USB_DCP           14B2<> 14D2<
USB_DDM           14B2<> 14D2<
USB_DDP           14B2<> 14C2<
USB_DEM           14B2<> 14C2< 37B2>
USB_DEP           14B2<> 14C2< 37B2>
USB_DFM           14B2<> 14B2< 37B2>
USB_DFP           14B2<> 14C2< 37B2>
USB_OC_AB_L       14B2< 14C7<
USB_OC_CD_L       14B2< 14C7<
USB_OC_EF_L       14B2< 14C7<
USB_PWREN_AB_L    14B2<> 14C7<
USB_PWREN_CD_L    14B2<> 14C7<
USB_PWREN_EF_L    14B2<> 14C7<
VCORE_AB_SEL      33A7<> 33C6<
VCORE_AB_SEL_INV  33A7<>
VCORE_AB_SEL_OPT  33A6<>
VCORE_BOOST       33C4<> 38C1>
VCORE_BST         33C5<> 38C1>
VCORE_CC          33B6<> 38C1>
VCORE_D0          33A3<>
VCORE_D1          33A3<>
VCORE_D2          33A3<>
VCORE_D3          33A3<>
VCORE_D4          33A3<>
VCORE_DH          33B5<> 38C1>
VCORE_DL          33B5<> 38C1>
VCORE_FAST<1>     33D4< 33D5<
VCORE_FAST<2>     33D4< 33D5<
VCORE_FAST<3>     33D4< 33D5<
VCORE_FAST<4>     33D4< 33D5<
VCORE_FB          33B5< 38B1> 39C6>
VCORE_GND         33B5<> 38B1>
VCORE_GNDA        33B6<> 38B1>
VCORE_GNDDIV      33A5< 33A5< 38B1>
VCORE_GNDDIV_TEST 33A4<>
VCORE_GNDSNS      33A1<> 33A5< 38B1>
VCORE_GNDSNS_TEST 33A4<>
VCORE_ILIM        33C6<> 38C1>
VCORE_LX          33B5<> 38C1>
VCORE_MUX_EN      33D5<>
VCORE_MUX_SEL     33D5<>
VCORE_OFFSET_DIV  33B6<>
VCORE_REF         33B6<> 38C1>
VCORE_SHDN_L      33C6<>
VCORE_SLOW<1>     33D6<
VCORE_SLOW<2>     33D6<
VCORE_SLOW<3>     33D6<
VCORE_SLOW<4>     33D6<
VCORE_SNS         33A1<> 38B1>
VCORE_TIME        33B4<> 38B1>
VCORE_TON         33B6< 38C1>
VCORE_VCC         33C6< 38C1>
VCORE_VGATE       14B5< 14B7< 33B4> 38B1>
VCORE_VID<0>      33B7<
VCORE_VID<1>      33B7< 33D3< 33D4>
VCORE_VID<2>      33B7< 33D3< 33D4>
VCORE_VID<3>      33B7< 33D3< 33D4>
VCORE_VID<4>      33B7< 33D3< 33D4>
VCORE_VSENSE      33C2<>
VGA_B             22C6<> 22C7< 39B6>
VGA_G             22C5<> 22C7< 39B6>
VGA_HSYNC         22C6<> 22D7< 39B6>
VGA_R             22B7< 22C5<> 39B6>
VGA_VSYNC         22C5<> 22D7< 39B6>
ZT10_SPN          4C2<>
ZT301_SPN         4C2<>
ZT302_SPN         4C2<>
ZV_LCDDATA20_PU   29C7<>
```


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SIZE	DRAWING NUMBER	REV.
D	051-6537	B
SCALE NONE	SHT 42 OF 44	

*** Part Cross-Reference for the entire design ***

C1	CAP	5
C2	CAP	5
C3	CAP	33
C4	CAP	33
C5	CAP	33
C6	CAP	33
C7	CAP	32
C8	CAP	32
C9	CAP	5
C10	CAP	5
C11	CAP	30
C12	CAP	33
C13	CAP	33
C14	CAP	33
C15	CAP	33
C16	CAP	33
C17	CAP	5
C18	CAP	5
C19	CAP	22
C20	CAP	5
C21	CAP	33
C22	CAP	22
C23	CAP	30
C24	CAP	30
C25	CAP	5
C26	CAP	5
C27	CAP	5
C28	CAP	5
C29	CAP	5
C30	CAP	5
C31	CAP	5
C32	CAP	5
C33	CAP	5
C34	CAP	5
C35	CAP	30
C36	CAP	30
C37	CAP	18
C38	CAP	5
C39	CAP	5
C40	CAP	18
C41	CAP	30
C42	CAP	30
C43	CAP	30
C44	CAP	5
C45	CAP	5
C46	CAP	5
C47	CAP	5
C48	CAP	5
C49	CAP	5
C50	CAP	5
C51	CAP_P	33
C52	CAP_P	33
C53	CAP	5
C54	CAP	5
C55	CAP	5
C56	CAP	5
C57	CAP	33
C58	CAP	5
C59	CAP	5
C60	CAP	18
C61	CAP	5
C62	CAP	5
C63	CAP	33
C64	CAP	33
C65	CAP	33
C66	CAP	33
C67	CAP	30
C68	CAP	5
C69	CAP	5
C70	CAP	33
C71	CAP	30
C72	CAP	5
C73	CAP	5
C74	CAP	33
C75	CAP	5
C76	CAP	33
C77	CAP_P	33
C78	CAP_P	33
C79	CAP	33
C80	CAP	33
C81	CAP	5
C82	CAP	5
C83	CAP	33
C84	CAP	33
C86	CAP	5
C87	CAP	5
C88	CAP	5
C89	CAP	5
C90	CAP	33
C91	CAP_P	33
C92	CAP_P	33
C93	CAP	33
C94	CAP	33
C95	CAP	30
C96	CAP	30
C97	CAP	30
C98	CAP	30
C99	CAP	30
C100	CAP	33
C101	CAP	33
C103	CAP	5
C104	CAP	5
C105	CAP	33
C106	CAP	33
C107	CAP	5
C108	CAP	5
C109	CAP	5
C110	CAP	5
C111	CAP_P	33
C112	CAP	30
C113	CAP	30
C114	CAP	32
C115	CAP	30
C116	CAP	30
C117	CAP	30
C118	CAP	30
C119	CAP	31
C120	CAP	6
C121	CAP	31
C122	CAP	9
C123	CAP	32
C124	CAP	31
C125	CAP	9
C126	CAP	32
C127	CAP	11
C128	CAP	11
C129	CAP	34
C130	CAP	33
C131	CAP	31
C132	CAP	11
C133	CAP	34
C134	CAP	31
C135	CAP	31
C136	CAP	17
C137	CAP	31
C138	CAP	31
C139	CAP	16
C140	CAP	11
C141	CAP	16
C142	CAP	16
C143	CAP	32
C144	CAP	16
C145	CAP	16
C146	CAP	16
C147	CAP	16
C148	CAP	16
C149	CAP	16
C150	CAP	11
C151	CAP	14
C152	CAP	14
C153	CAP	31
C154	CAP	31
C155	CAP	31
C156	CAP	11
C157	CAP	11
C158	CAP	16
C159	CAP	16
C160	CAP	16
C161	CAP	16
C162	CAP	16
C163	CAP	16
C164	CAP	16
C165	CAP	16
C166	CAP	16
C167	CAP	16
C168	CAP	16
C169	CAP	11
C170	CAP	16
C171	CAP	16
C172	CAP	16
C173	CAP	17
C174	CAP	11
C175	CAP	16
C176	CAP	16
C177	CAP	16
C178	CAP	16
C179	CAP	16
C180	CAP	16
C181	CAP	16
C182	CAP	16
C183	CAP	16
C184	CAP	16
C185	CAP	16
C186	CAP	16
C187	CAP	8
C188	CAP	23
C189	CAP	16
C190	CAP	12
C191	CAP	16
C192	CAP	16
C193	CAP	34
C194	CAP	34
C195	CAP	34
C196	CAP	34
C197	CAP	17
C198	CAP	23
C199	CAP	23
C200	CAP	16
C201	CAP	16
C202	CAP	16
C203	CAP	16
C204	CAP	16
C205	CAP	16
C206	CAP	16
C207	CAP	16
C208	CAP	16
C209	CAP	34
C210	CAP	23
C211	CAP	11
C212	CAP	16
C213	CAP	16
C214	CAP	16
C215	CAP	16
C216	CAP	16
C217	CAP	16
C218	CAP	16
C219	CAP	16
C220	CAP	23
C221	CAP	16
C222	CAP	16
C223	CAP	16
C224	CAP	16
C225	CAP	16
C226	CAP	16
C227	CAP	16
C228	CAP	16
C229	CAP	16
C230	CAP	16
C231	CAP	16
C232	CAP	34
C233	CAP	23
C234	CAP	16
C235	CAP	14
C236	CAP	16
C237	CAP	16
C238	CAP	16
C239	CAP	16
C240	CAP	16
C241	CAP	16
C242	CAP	16
C243	CAP	16
C244	CAP	31
C245	CAP	16
C246	CAP	14
C247	CAP	16
C248	CAP	16
C249	CAP	9
C250	CAP	16
C251	CAP	16
C252	CAP	16
C253	CAP	16
C254	CAP	16
C255	CAP	29
C256	CAP	14
C257	CAP	16
C258	CAP	16
C259	CAP	16
C260	CAP	16
C261	CAP	16
C262	CAP	16
C263	CAP	16
C264	CAP	16
C265	CAP	16
C266	CAP	16
C267	CAP_P	34
C268	CAP	16
C269	CAP	16
C270	CAP	12
C271	CAP	16
C272	CAP	16
C273	CAP	16
C274	CAP	16
C275	CAP	16
C276	CAP	31
C277	CAP	29
C278	CAP	16
C279	CAP	16
C280	CAP	16
C281	CAP	16
C282	CAP	16
C283	CAP	16
C284	CAP	24
C285	CAP	16
C286	CAP	16
C287	CAP	16
C288	CAP	16
C289	CAP	16
C290	CAP	16
C291	CAP	12
C292	CAP	16
C293	CAP	16
C294	CAP	16
C295	CAP	16
C296	CAP	16
C297	CAP	16
C298	CAP	34
C299	CAP	16
C300	CAP	16
C301	CAP	16
C302	CAP	16
C303	CAP	16
C304	CAP	16
C305	CAP	16
C306	CAP	16
C307	CAP_P	34
C308	CAP	16
C309	CAP	16
C310	CAP	16
C311	CAP	12
C312	CAP	16
C313	CAP	16
C314	CAP	16
C315	CAP	16
C316	CAP	16
C317	CAP	16
C318	CAP	16
C319	CAP	16
C320	CAP	16
C321	CAP	16
C322	CAP	16
C323	CAP	16
C324	CAP	16
C325	CAP	16
C326	CAP	31
C327	CAP	16
C328	CAP	16
C329	CAP	16
C330	CAP	16
C331	CAP	16
C332	CAP	16
C333	CAP	16
C334	CAP	16
C335	CAP	16
C336	CAP	31
C337	CAP	14
C338	CAP	34
C339	CAP	29
C340	CAP	29
C341	CAP	16
C342	CAP	16
C343	CAP	16
C344	CAP	16
C345	CAP	16
C346	CAP	16
C347	CAP	16
C348	CAP	16
C349	CAP	16
C350	CAP	16
C351	CAP	16
C352	CAP	16
C353	CAP	32
C354	CAP	16
C355	CAP	34
C356	CAP	11
C357	CAP	16
C358	CAP	16
C359	CAP	16
C360	CAP	16
C361	CAP	16
C362	CAP	12
C363	CAP	16
C364	CAP	16
C365	CAP	16
C366	CAP	16
C367	CAP	16
C368	CAP	16
C369	CAP	16
C370	CAP	29
C371	CAP	16
C372	CAP	12
C373	CAP	16
C374	CAP	16
C375	CAP	16
C376	CAP	16
C377	CAP	16
C378	CAP	16
C379	CAP	16
C380	CAP	16
C381	CAP	16
C382	CAP	16
C383	CAP	11
C384	CAP	19
C385	CAP	16
C386	CAP	14
C387	CAP	14
C388	CAP	14
C389	CAP	14
C390	CAP	19
C391	CAP	11
C392	CAP	14
C393	CAP_P	34
C394	CAP	14
C395	CAP	16
C396	CAP_P	34
C397	CAP	11
C398	CAP	32
C399	CAP	14
C400	CAP	14
C401	CAP	19
C402	CAP	14
C403	CAP	11
C404	CAP	11
C405	CAP_P	34
C406	CAP	29
C407	CAP	20
C408	CAP	19
C409	CAP	19
C410	CAP	32
C411	CAP	20
C412	CAP	19
C413	CAP	21
C414	CAP	21
C415	CAP	32
C416	CAP	32
C417	CAP	21
C418	CAP	21
C419	CAP	21
C420	CAP	21
C421	CAP	21
C422	CAP	21
C423	CAP	21
C424	CAP	21
C425	CAP	21
C426	CAP	21
C427	CAP	21
C428	CAP	32
C429	CAP	32
C430	CAP	21
C431	CAP	20
C432	CAP	32
C433	CAP	32
C434	CAP	20
C435	CAP	20
C436	CAP	21
C437	CAP	21
C438	CAP	21
C439	CAP	21
C440	CAP	20
C441	CAP	20
C442	CAP	19
C443	CAP	20
C444	CAP	21
C445	CAP	20
C446	CAP	20
C447	CAP	21
C448	CAP	20
C449	CAP	20
C450	CAP	21
C451	CAP	20
C452	CAP	20
C453	CAP	21
C454	CAP	21
C455	CAP	20
C456	CAP	21
C457	CAP	19
C458	CAP	19
C459	CAP	21
C460	CAP	21
C461	CAP	21
C462	CAP	21
C463	CAP	21
C464	CAP	21
C465	CAP	20
C466	CAP	20
C467	CAP	29
C468	CAP	21
C469	CAP	20
C470	CAP	21
C471	CAP	21
C472	CAP	21
C473	CAP	21
C474	CAP	22
C475	CAP	21
C476	CAP	19
C477	CAP	20
C478	CAP	21
C479	CAP	20
C480	CAP	20
C481	CAP	20
C482	CAP	20
C483	CAP	21
C484	CAP	20
C485	CAP	20
C486	CAP	20
C487	CAP	20
C488	CAP	21
C489	CAP	21
C490	CAP	19
C491	CAP	21
C492	CAP	21
C493	CAP	21
C494	CAP	20
C495	CAP	20
C496	CAP	21
C497	CAP	20
C498	CAP	20
C499	CAP	21
C500	CAP	21
C501	CAP	21
C503	CAP	22
C504	CAP	21
C505	CAP	20
C506	CAP	21
C507	CAP	20
C508	CAP	19
C509	CAP	20
C510	CAP	20
C511	CAP	21
C512	CAP	20
C513	CAP	20
C514	CAP	21
C515	CAP	20
C516	CAP	19
C517	CAP	21
C518	CAP	21
C519	CAP	21
C520	CAP	21
C521	CAP	21
C522	CAP	20
C523	CAP	21
C524	CAP	20
C525	CAP	20
C526	CAP	20
C527	CAP	21
C528	CAP	20
C529	CAP	20
C530	CAP	19
C531	CAP	20
C532	CAP	20
C533	CAP	20
C534	CAP	21
C535	CAP	21
C536	CAP	20
C537	CAP	21
C538	CAP	21
C539	CAP	21
C540	CAP	21
C541	CAP	21
C542	CAP	21
C543	CAP	21
C544	CAP	21
C545	CAP	21
C546	CAP	21
C547	CAP	21
C548	CAP	22
C549	CAP	22
C550	CAP	21
C551	CAP	21
C552	CAP	21
C553	CAP	21
C554	CAP	32
C555	CAP	32
C556	CAP	32
C557	CAP	32
C558	CAP	32
C559	CAP	32
C560	CAP	32
C561	CAP	32
C562	CAP	32
C563	CAP	32
C564	CAP	32
C565	CAP	32
C566	CAP	32
C567	CAP	32
C568	CAP	32
C569	CAP	32
C570	CAP	32
C571	CAP	32
C572	CAP	32
C573	CAP	32
C574	CAP	32
C575	CAP	32
C576	CAP	32
C577	CAP	32
C578	CAP	32
C579	CAP	32
C580	CAP	32
C581	CAP	32
C582	CAP	32
C583	CAP	27
C584	CAP	27
C585	CAP	27
C586	CAP	27
C587	CAP	27
C588	CAP	27
C589	CAP	27
C590	CAP	27
C591	CAP	27
C592	CAP	26
C593	CAP	27
C594	CAP	26
C595	CAP	26
C596	CAP	27
C597	CAP	26
C598	CAP	26
C599	CAP	26
C600	CAP	26
C601	CAP	26
C602	CAP	26
C603	CAP	26
C604	CAP	26
C605	CAP	27
C606	CAP	27
C607	CAP	27
C608	CAP	26
C609	CAP	27
C610	CAP	27
C611	CAP	26
C612	CAP	26
C613	CAP	26
C614	CAP	26
C615	CAP	26
C616	CAP	26
C617	CAP	26
C618	CAP	26
C619	CAP	26
C620	CAP	27
C621	CAP	27
C622	CAP	26
C623	CAP	26
C624	CAP	26
C625	CAP	27
C627	CAP	32
C628	CAP	32
C629	CAP	32
C630	CAP	28
C631	CAP	22
C632	CAP	22
C633	CAP	28
C634	CAP	22
C635	CAP	22
C637	CAP	28
C638	CAP	28
C639	CAP	28
C640	CAP	28
C641	CAP	22
C642	CAP	22
C644	CAP	28
C645	CAP	26
C646	CAP	26
C647	CAP	26
C648	CAP	26
C649	CAP	28
C650	CAP	28
C651	CAP	28
C652	CAP	28
C653	CAP	22
C654	CAP	22
C655	CAP	22
C656	CAP	22
C657	CAP	22
C658	CAP	22
C659	CAP	22
C660	CAP	22
C661	CAP	22
C662	CAP	28
C663	CAP	22
C664	CAP	22
C665	CAP	27
C666	CAP	28
C667	CAP	22
C668	CAP	22
C669	CAP	25
C670	CAP_P	27
C671	CAP	27
C672	CAP	27
C673	CAP	27
C674	CAP	26
C675	CAP	26
C676	CAP	27
C677	CAP	27
C678	CAP	27
C679	CAP	27
C680	CAP	26
C681	CAP	27
C682	CAP	27
C683	CAP	27
C684	CAP	27
C685	CAP_P	32
C686	CAP	32
C687	CAP	32
C688	CAP	32
C689	CAP	25
C690	CAP	34
C691	CAP	34
C692	CAP	25
C693	CAP	34
C694	CAP	32
C695	CAP	34
C696	CAP	25
C697	CAP	34
C698	CAP	25
C699	CAP	32
C700	CAP	32
C701	CAP	22
C702	CAP	22
C703	CAP_P	32
C704	CAP	20
C705	CAP_P	20
C706	CAP	20
C707	CAP_P	20
C708	CAP	20
C709	CAP_P	32
C710	CAP_P	32
C711	CAP_P	20
C712	CAP	20
C713	CAP_P	32
C714	CAP	34
C715	CAP	34
C716	CAP	34
C717	CAP	34
C718	CAP	34
C719	CAP	34
C720	CAP	34
C721	CAP	14
C722	CAP	34
C723	CAP	14
C724	CAP	29
C725	CAP	34
C726	CAP	10
C727	CAP	10
C728	CAP	29
C729	CAP	29
C730	CAP	10
C731	CAP	29
C732	CAP	10
C733	CAP	10
C734	CAP	10
C735	CAP	16
C736	CAP	16
C737	CAP	31
C738	CAP	34
C739	CAP	16
C740	CAP	31
C741	CAP	10
C742	CAP	10
C743	CAP	17
C744	CAP	17
C745	CAP	10
C746	CAP	17
C747	CAP	17
C748	CAP	17
C749	CAP	17
C750	CAP	17
C751	CAP	17
C752	CAP	17
C753	CAP	31
C754	CAP	31
C755	CAP	31
C756	CAP	17
C757	CAP	10
C758	CAP	10
C759	CAP	17
C760	CAP	17
C761	CAP	17
C762	CAP	6
C763	CAP	25
C764	CAP	10
C765	CAP	17
C766	CAP	23
C767	CAP	31
C768	CAP	17
C769	CAP	17
C770	CAP	16
C771	CAP	31
C772	CAP	31
C773	CAP	9
C774	CAP_P	33
C775	CAP	18
C776	CAP	18
C777	CAP	30
C778	CAP	18
C779	CAP_P	30
C780	CAP	30
C781	CAP_P	33
C782	CAP	18
C783	CAP	18
C784	CAP	18
C785	CAP	30
C786	CAP	18
C787	CAP	18
C788	CAP_P	33
C789	CAP	18
C790	CAP	30
C791	CAP	18
C792	CAP	30
C793	CAP_P	33
C794	CAP	30
C795	CAP	30
C796	CAP	18
C797	CAP_P	33
C798	CAP	30
C799	CAP	30
C800	CAP	18
C801	CAP	30
C802	CAP_P	33
C803	CAP	30
C804	CAP_P	31
C805	CAP	24
C806	CAP_P	31
C807	CAP	30
C808	CAP	24
C809	CAP	30
C810	CAP	5
C811	CAP	5
C812	CAP	22
C813	CAP	22
C814	CAP	25
C815	CAP	22
C816	CAP	22
C817	CAP	25
C818	CAP	25
C819	CAP	22
C826	CAP	30
C828	CAP	25
C829	CAP	25
C830	CAP	21
C831	CAP	21
C832	CAP	21
C833	CAP	21
C834	CAP	21
C835	CAP	21
C838	CAP	20
C839	CAP	32
C840	CAP	32
C841	CAP	33
C842	CAP	33
C843	CAP	33
C844	CAP	34
C845	CAP	34
C846	CAP	20
C847	CAP	13
C848	CAP_P	25
C849	CAP	25
C850	CAP	25
C851	CAP	26
C852	CAP	26
C853	CAP	30
C854	CAP	19
C855	CAP	19
C856	CAP	19
C857	CAP	19
C858	CAP	19
C859	CAP	19
C860	CAP	19
C861	CAP	19
C862	CAP	19
C863	CAP	19
C864	CAP	19
C865	CAP	19
C866	CAP	19
C867	CAP	19
C868	CAP	25
C869	CAP	25
C871	CAP	19
C872	CAP	19
C873	CAP	19
C874	CAP	19
C875	CAP	19
C876	CAP	19
C877	CAP	19
C878	CAP	19
C879	CAP	19
C880	CAP	21
C881	CAP	21
D1	DIODE_SCHOT	31
D2	DIODE_SCHOT	31
D3	DIODE	31
D4	DIODE	30
D5	DIODE_SCHOT	33
D6	DIODE	30
D7	DIODE_SCHOT	31
D8	DIODE	31
D9	ZENER_MMBZ15VDLT1	23
D10	DIODE_SCHOT	31
D11	DIODE_SCHOT	31
D12	DIODE	20
D13	DIODE_SCHOT	32
D14	DIODE_SCHOT	32
D15	DIODE	26
D16	DIODE_SCHOT	27
D18	DIODE_DUAL_6P	28
D19	DIODE_SCHOT	22
D20	DIODE_DUAL_6P	28
D21	ZENER	28
D22	DIODE_DUAL_6P	28
D23	DIODE_DUAL_6P	28
D24	DIODE_SCHOT	28
D25	DIODE_SCHOT_3P2	27
D26	DIODE_SCHOT	32
D27	DIODE	32
D28	DIODE_SCHOT	32
D29	DIODE_SCHOT	20
D30	DIODE_SCHOT	34
D31	DIODE_SCHOT	34
D32	DIODE_SCHOT	31
D33	DIODE	33
D36	DIODE_SCHOT	30
DP1	DPAK3P	30
DP2	DPAK3P	33
DP3	DPAK3P	34
DP4	DPAK3P	34
DP5	DPAK3P	20
DP6	DPAK3P	28
DP7	DPAK3P	20
F1	FUSE	28
F2	FUSE	22
F3	FUSE	28
F4	FUSE	30
F5	FUSE	30
G1	OSC	19
G2	OSC	27
J1	CON_M4RT_S2MT_SM	25
J2	CON_4RT_WRIB	23
J3	CON_M40ST_D4MT_SM	25
J4	CON_4RT_WRIB	22
J5	CON_M80ST_D4MT_SM	18
J6	CON_F80ST_D4MT_SM	24
J7	CON_12	33
J8	CON_2RTSM_125	23
J9	CON_F1ST_S2MT_SM	14
J10	CON_10STSM_5087	23
J11	CON_F30RT_S2MT_SM1	23
J12	CON_M50SM_5MM	24
J13	CON_M50SM_5MM	24
J14	CON_F30RT_S2MT_SM	22
J15	CON_M16ST_D_SMA	25
J16	CON_3RTSM_125	31
J17	CON_M16ST_D_SMA	25
J18	CON_M4RT_S2MT_SM	25
J19	CON_F20ST_D_SM	23
J20	CON_F9RT_1394B_S6MT_SMA	28
J21	CON_F5RT_MINIDIN_TH	22
J22	CON_F30RT_T6MT_TH1	22
J23	CON_RJ45_10RT_S4MT_TH1	26
J24	CON_F6RT_S4MT_TH1	28
J25	CON_F400RT_DDRDIMM_SM3	11
J26	CON_M8RT_S_SM	30
J27	CON_M4RT_S_SM	30
J28	CON_10STSM_5087	25
L1	IND	22
L2	IND	30
L3	IND	30
L4	IND	30
L5	IND	30
L6	IND	30
L7	IND	17
L8	IND	23
L9	IND	23
L10	IND	23
L11	IND	23
L12	IND	23
L13	IND	14
L14	IND	14
L15	IND	14
L16	IND	19
L17	IND	20
L18	IND	21
L19	IND	21
L20	IND	21
L21	IND	21
L22	IND	19
L23	IND	21
L24	IND	21
L25	IND	21
L26	IND	21
L27	IND	22
L28	IND	21
L29	IND	21
L30	IND	21
L31	IND	21
L32	IND	21
L33	IND	21
L34	IND	27
L35	IND	26
L36	IND	22
L37	FILTER_4P	22
L38	IND	22
L39	IND	28
L40	IND	22
L41	IND	22
L42	IND	22
L43	IND	22
L44	IND	22
L45	FILTER_4P	22
L46	FILTER_4P	22
L47	FILTER_4P	22
L48	FILTER_4P	28
L49	IND	22
L50	IND	22
L51	IND	28
L52	FILTER_4P	28
L53	IND	22
L54	IND	22
L55	IND	22
L56	IND	22
L57	IND	22
L58	IND	28
L59	IND	27
L60	IND	26
L61	IND	32
L62	IND	32
L63	IND	34
L64	IND_3P	20
L65	IND	34
L66	IND	19
L67	IND	34
L68	IND	23
L69	IND_3P	31
L70	IND	30
L71	IND_3P	33
L72	IND	22
L73	IND	22
L74	IND	22
L75	IND	21
L76	FILTER_4P	28
L77	FILTER_4P	28
L78	IND	19
L79	IND	19
L80	IND	19
L81	IND	21
Q1	TRA_2N7002DW	30
Q2	TRA_2N7002DW	30
Q3	TRA_2N7002DW	7
Q4	TRA_2N7002DW	30
Q5	TRA_2N3904	33
Q6	TRA_SI4435DY	30
Q7	TRA_SUD45P03	30
Q8	TRA_2N3904	33
Q9	TRA_2N7002DW	30
Q10	TRA_2N7002	34
Q11	TRA_2N7002DW	34
Q12	TRA_2N3904	7
Q13	TRA_2N7002	7
Q14	TRA_2N7002DW	7
Q15	TRA_FDG6324L	31
Q16	TRA_IRF7811W	31
Q17	TRA_IRF7805	31
Q18	TRA_2N7002DW	23
Q19	TRA_2N3906	23
Q20	TRA_2N7002DW	32
Q21	TRA_SI3443DV	32
Q22	TRA_2N3906	23
Q23	TRA_SI3446DV	20
Q24	TRA_2N7002DW	32
Q25	TRA_2N7002DW	20
Q26	TRA_SI3443DV	32
Q27	TRA_SI3443DV	32
Q28	TRA_2N7002	22
Q29	TRA_SI3443DV	22
Q30	TRA_2N7002	29
Q31	TRA_2N7002	34
Q32	TRA_2N7002DW	26
Q33	TRA_2N7002DW	28
Q34	TRA_NDS9407	28
Q35	TRA_DUAL_MMDT3904	22
Q38	TRA_TP0610	22
Q39	TRA_2N7002DW	22
Q40	TRA_2N7002DW	22
Q41	TRA_SI4888DY	32
Q42	TRA_SI4888DY	32
Q43	TRA_2N7002	32
Q44	TRA_2N7002DW	32
Q45	TRA_SI4888DY	32
Q46	TRA_2N3904	25
Q47	TRA_SI4888DY	32
Q48	TRA_SI7860DP	20
Q49	TRA_IRF7832	20
Q50	TRA_2N7002DW	32
Q51	TRA_2N3904	20
Q52	TRA_2N3904	20
Q53	TRA_SI3446DV	34
Q54	TRA_IRF7811W	34
Q55	TRA_IRF7805	34
Q56	TRA_IRF7805	34
Q57	TRA_IRF7811W	34
Q58	TRA_2N3906	23
Q59	TRA_2N3904	25
Q60	TRA_IRF7832	33
Q61	TRA_2N3904	25
Q62	TRA_SI7860DP	33
Q63	TRA_IRF7832	33
Q64	TRA_IRF7811W	30
Q65	TRA_SI7860DP	33
Q66	TRA_IRF7832	33
Q67	TRA_2N3904	25
Q68	TRA_SI4435DY	30
Q69	TRA_SI4435DY	30
Q70	TRA_IRF7805	30
Q71	TRA_2N7002DW	30
Q72	TRA_2N7002DW	30
Q74	TRA_2N7002DW	30
Q76	TRA_FDG6324L	22
Q77	TRA_2N7002DW	25
Q78	TRA_2N7002DW	25
Q79	TRA_2N7002DW	25
Q82	TRA_2N7002DW	33
Q83	TRA_2N7002DW	25
R2	RES	5
R3	RES	5
R4	RES	5
R5	RES	7
R6	RES	5
R7	RES	5
R8	RES	5
R9	RES	5
R10	RES	5
R11	RES	5
R12	RES	7
R13	RES	5
R14	RES	7
R15	RES	30
R16	RES	30
R17	RES	7
R18	RES	7
R19	RES	5
R20	RES	5
R21	RES	30
R22	RES	30
R23	RES	7
R24	RES	5
R25	RES	5
R26	RES	5
R27	RES	5
R28	RES	5
R29	RES	30
R30	RES	30
R31	RES	7
R32	RES	5
R33	RES	5
R34	RES	5
R35	RES	7
R36	RES	5
R37	RES	5
R38	RES	5
R39	RES	31
R40	RES	30
R41	RES	30
R42	RES	30
R43	RES	7
R44	RES	7
R45	RES	5
R46	RES	5
R47	RES	30
R48	RES	7
R49	RES	30
R50	RES	7
R51	RES	30
R52	RES	30
R53	RES	30
R54	RES	30
R55	RES	30
R56	RES	30
R57	RES	30
R58	RES	30
R59	RES	30
R60	RES	7
R61	RES	30
R62	RES	30
R63	RES	7
R64	RES	7
R65	RES	33
R66	RES	33
R67	RES	33
R68	RES	7
R69	RES	33
R70	RES	7
R71	RES	33
R72	RES	33
R73	RES	30
R74	RES	30
R75	RES	30
R76	RES	7
R77	RES	30
R78	RES	7
R79	RES	7
R80	RES	33
R81	RES	33
R82	RES	30
R83	RES	30
R84	RES	7
R85	RES	33
R86	RES	33
R87	RES	30
R88	RES	7
R89	RES	5
R90	RES	33
R91	RES	33
R92	RES	7
R93	RES	33
R94	RES	30
R95	RES	33
R96	RES	30
R97	RES	33
R98	RES	33
R99	RES	33
R100	RES	6
R101	RES	33
R102	RES	30
R103	RES	6
R104	RES	6
R105	RES	6
R106	RES	33
R107	RES	31
R108	RES	31
R109	RES	31
R110	RES	7
R111	RES	33
R112	RES	9
R113	RES	14
R114	RES	34
R115	RES	34
R116	RES	34
R117	RES	34
R118	RES	31
R119	RES	30
R120	RES	31
R121	RES	33
R122	RES	31
R123	RES	33
R124	RES	17
R125	RES	33
R126	RES	33
R127	RES	31
R128	RES	8
R129	RES	33
R130	RES	31
R131	RES	7
R132	RES	7
R133	RES	7
R134	RES	14
R135	RES	33
R136	RES	8
R137	RES	33
R138	RES	23
R139	RES	33
R140	RES	8
R141	RES	8
R142	RES	14
R143	RES	14
R144	RES	14
R145	RES	13
R146	RES	8
R147	RES	8
R148	RES	14
R149	RES	13
R150	RES	8
R151	RES	8
R152	RES	8
R153	RES	14
R154	RES	23
R155	RES	8
R156	RES	14
R157	RES	14
R158	RES	14
R159	RES	8
R160	RES	13
R161	RES	8
R162	RES	9
R163	RES	23
R164	RES	14
R165	RES	14
R166	RES	14
R167	RES	12
R168	RES	8
R169	RES	8
R170	RES	34
R171	RES	34
R172	RES	17
R173	RES	23
R174	RES	14
R175	RES	14
R176	RES	9
R177	RES	34
R178	RES	14
R179	RES	14
R180	RES	14
R181	RES	14
R182	RES	14
R183	RES	14
R184	RES	34
R185	RES	23
R186	RES	13
R187	RES	14
R188	RES	14
R189	RES	14
R190	RES	23
R191	RES	14
R192	RES	14
R193	RES	14
R195	RES	13
R196	RES	24
R197	RES	12
R198	RES	23
R199	RES	24
R200	RES	24
R201	RES	14
R202	RES	9
R203	RES	24
R204	RES	24
R205	RES	13
R206	RES	14
R207	RES	13
R208	RES	9
R209	RES	9
R210	RES	34
R211	RES	34
R212	RES	34
R213	RES	24
R214	RES	24
R215	RES	24
R216	RES	24
R217	RES	24
R218	RES	14
R219	RES	12
R220	RES	34
R221	RES	34
R222	RES	34
R223	RES	23
R224	RES	13
R225	RES	12
R226	RES	34
R227	RES	34
R228	RES	23
R229	RES	24
R230	RES	12
R231	RES	31
R232	RES	13
R233	RES	31
R234	RES	24
R235	RES	12
R237	RES	24
R238	RES	24
R239	RES	12
R240	RES	14
R241	RES	14
R242	RES	24
R243	RES	14
R244	RES	12
R245	RES	12
R246	RES	12
R247	RES	9
R248	RES	29
R249	RES	29
R250	RES	14
R251	RES	24
R252	RES	12
R253	RES	12
R254	RES	12
R255	RES	12
R256	RES	12
R257	RES	9
R258	RES	14
R259	RES	13
R260	RES	9
R261	RES	29
R262	RES	24
R263	RES	13
R264	RES	12
R265	RES	9
R266	RES	24
R267	RES	29
R268	RES	24
R269	RES	13
R270	RES	13
R272	RES	12
R273	RES	12
R274	RES	15
R275	RES	21
R276	RES	15
R277	RES	12
R278	RES	12
R279	RES	14
R280	RES	14
R281	RES	5
R282	RES	12
R283	RES	5
R284	RES	14
R285	RES	19
R286	RES	14
R287	RES	14
R288	RES	14
R289	RES	19
R290	RES	19
R291	RES	32
R292	RES	14
R293	RES	14
R294	RES	32
R295	RES	14
R296	RES	14
R297	RES	19
R298	RES	19
R299	RES	11
R300	RES	23
R301	RES	32
R303	RES	11
R304	RES	19
R305	RES	19
R306	RES	32
R307	RES	32
R308	RES	12
R309	RES	19
R310	RES	32
R311	RES	32
R312	RES	21
R313	RES	19
R314	RES	12
R315	RES	19
R316	RES	12
R317	RES	12
R318	RES	12
R319	RES	21
R320	RES	19
R321	RES	32
R322	RES	32
R323	RES	19
R324	RES	19
R325	RES	19
R326	RES	20
R327	RES	20
R328	RES	20
R329	RES	20
R330	RES	20
R331	RES	20
R332	RES	20
R333	RES	20
R334	RES	12
R335	RES	19
R336	RES	19
R337	RES	19
R338	RES	19
R339	RES	20
R340	RES	20
R341	RES	20
R342	RES	20
R343	RES	20
R344	RES	20
R345	RES	29
R346	RES	20
R347	RES	22
R348	RES	29
R349	RES	29
R350	RES	20
R351	RES	20
R352	RES	20
R353	RES	20
R354	RES	22
R355	RES	20
R356	RES	20
R357	RES	20
R358	RES	20
R359	RES	20
R360	RES	20
R361	RES	20
R362	RES	20
R363	RES	21
R364	RES	29
R365	RES	19
R366	RES	20
R367	RES	20
R368	RES	20
R369	RES	20
R370	RES	19
R371	RES	19
R372	RES	19
R373	RES	19
R374	RES	20
R375	RES	19
R376	RES	19
R377	RES	20
R378	RES	20
R379	RES	21
R380	RES	20
R381	RES	20
R382	RES	20
R383	RES	20
R384	RES	20
R385	RES	20
R386	RES	20
R387	RES	20
R388	RES	19
R389	RES	20
R390	RES	20
R391	RES	20
R392	RES	20
R393	RES	20
R394	RES	20
R395	RES	20
R396	RES	20
R397	RES	19
R398	RES	34
R399	RES	32
R400	RES	32
R401	RES	32
R402	RES	32
R403	RES	32
R404	RES	32
R405	RES	32
R406	RES	32
R407	RES	32
R408	RES	32
R409	RES	32
R410	RES	32
R411	RES	32
R412	RES	27
R413	RES	27
R414	RES	27
R415	RES	27
R416	RES	27
R417	RES	27

R418	RES	27
R419	RES	27
R420	RES	27
R421	RES	26
R422	RES	26
R423	RES	26
R424	RES	26
R425	RES	26
R426	RES	27
R427	RES	26
R428	RES	26
R429	RES	26
R430	RES	26
R431	RES	26
R432	RES	26
R433	RES	26
R434	RES	26
R435	RES	26
R436	RES	26
R437	RES	26
R438	RES	26
R439	RES	26
R440	RES	26
R441	RES	26
R442	RES	26
R443	RES	27
R444	RES	27
R445	RES	26
R446	RES	28
R447	RES	28
R448	RES	28
R451	RES	28
R454	RES	25
R456	RES	22
R458	RES	22
R459	RES	22
R460	RES	22
R461	RES	28
R462	RES	22
R463	RES	22
R464	RES	22
R465	RES	28
R466	RES	28
R469	RES	22
R470	RES	22
R471	RES	28
R472	RES	22
R473	RES	22
R474	RES	22
R475	RES	22
R476	RES	22
R477	RES	22
R478	RES	22
R479	RES	22
R480	RES	22
R481	RES	22
R482	RES	22
R483	RES	22
R484	RES	22
R485	RES	22
R486	RES	27
R487	RES	27
R488	RES	27
R489	RES	27
R490	RES	27
R491	RES	27
R492	RES	27
R493	RES	27
R494	RES	27
R495	RES	27
R496	RES	27
R497	RES	27
R498	RES	27
R499	RES	27
RS00	RES	27
RS01	RES	27
RS02	RES	27
RS03	RES	26
RS04	RES	26
RS05	RES	27
RS06	RES	26
RS07	RES	26
RS08	RES	27
RS09	RES	27
RS10	RES	27
RS11	RES	27
RS12	RES	27
RS13	RES	26
RS14	RES	27
RS15	RES	27
RS16	RES	27
RS17	RES	27
RS18	RES	27
RS19	RES	27
RS20	RES	27
RS21	RES	32
RS22	RES	32
RS23	RES	32
RS24	RES	32
RS25	RES	34
RS26	RES	34
RS27	RES	34
RS28	RES	34
RS29	RES	34
RS30	RES	25
RS31	RES	34
RS32	RES	34
RS33	RES	32
RS34	RES	32
RS35	RES	34
RS36	RES	34
RS37	RES	32
RS38	RES	32
RS39	RES	32
RS40	RES	24
RS41	RES	24
RS42	RES	24
RS43	RES	22
RS44	RES	22
RS45	RES	24
RS46	RES	24
RS47	RES	25
RS48	RES	32
RS49	RES	20
RS50	RES	32
RS51	RES	32
RS52	RES	12
RS53	RES	12
RS54	RES	34
RS55	RES	20
RS56	RES	20
RS57	RES	34
RS58	RES	20
RS59	RES	20
RS60	RES	29
RS61	RES	29
RS62	RES	29
RS63	RES	29
RS64	RES	29
RS65	RES	14
RS66	RES	34
RS67	RES	14
RS68	RES	14
RS69	RES	23
RS70	RES	24
RS71	RES	34
RS72	RES	32
RS73	RES	24
RS74	RES	14
RS75	RES	29
RS76	RES	29
RS77	RES	23
RS78	RES	24
RS79	RES	24
RS80	RES	29
RS81	RES	29
RS82	RES	29
RS83	RES	29
RS84	RES	29
RS85	RES	29
RS86	RES	29
RS87	RES	29
RS88	RES	29
RS89	RES	29
RS90	RES	29
RS91	RES	29
RS92	RES	29
RS93	RES	29

RS94	RES	29
RS95	RES	29
RS96	RES	29
RS97	RES	29
RS98	RES	29
RS99	RES	29
R600	RES	29
R602	RES	29
R603	RES	23
R604	RES	31
R605	RES	31
R606	RES	17
R607	RES	17
R608	RES	17
R609	RES	17
R610	RES	17
R611	RES	23
R612	RES	17
R613	RES	17
R614	RES	17
R615	RES	17
R616	RES	23
R617	RES	17
R618	RES	8
R619	RES	8
R620	RES	8
R621	RES	8
R622	RES	8
R623	RES	8
R624	RES	8
R625	RES	8
R626	RES	8
R627	RES	8
R628	RES	8
R629	RES	8
R631	RES	33
R632	RES	17
R633	RES	25
R634	RES	33
R635	RES	33
R636	RES	17
R637	RES	6
R638	RES	8
R639	RES	8
R640	RES	8
R641	RES	8
R642	RES	8
R643	RES	8
R644	RES	8
R645	RES	8
R646	RES	8
R647	RES	33
R648	RES	8
R649	RES	8
R650	RES	8
R651	RES	8
R652	RES	8
R653	RES	8
R654	RES	8
R655	RES	8
R656	RES	8
R657	RES	8
R658	RES	8
R659	RES	25
R660	RES	33
R661	RES	25
R662	RES	33
R663	RES	31
R664	RES	8
R665	RES	8
R666	RES	8
R667	RES	8
R668	RES	8
R669	RES	8
R670	RES	8
R671	RES	33
R672	RES	33
R673	RES	31
R674	RES	9
R675	RES	33
R676	RES	33
R677	RES	8
R678	RES	8
R679	RES	8
R680	RES	8
R681	RES	8
R682	RES	8
R683	RES	8
R684	RES	8
R685	RES	8
R686	RES	25
R687	RES	25
R688	RES	25
R689	RES	25
R690	RES	31
R691	RES	9
R692	RES	6
R693	RES	8
R694	RES	8
R695	RES	8
R696	RES	8
R697	RES	8
R698	RES	8
R699	RES	8
R700	RES	25
R701	RES	25
R702	RES	25
R703	RES	25
R704	RES	25
R705	RES	25
R706	RES	33
R707	RES	6
R708	RES	33
R709	RES	6
R710	RES	30
R711	RES	30
R712	RES	6
R713	RES	30
R714	RES	18
R715	RES	30
R716	RES	30
R717	RES	30
R718	RES	18
R719	RES	18
R720	RES	30
R721	RES	18
R722	RES	18
R723	RES	18
R724	RES	18
R725	RES	30
R726	RES	18
R727	RES	30
R728	RES	30
R729	RES	30
R730	RES	30
R731	RES	30
R732	RES	30
R733	RES	30
R734	RES	30
R735	RES	30
R736	RES	30
R737	RES	24
R738	RES	30
R739	RES	24
R740	RES	30
R741	RES	30
R742	RES	30
R743	RES	33
R744	RES	30
R745	RES	30
R746	RES	14
R747	RES	24
R748	RES	5
R749	RES	25
R750	RES	22
R751	RES	25
R752	RES	25
R753	RES	22
R754	RES	23
R757	RES	33
R760	RES	20
R761	RES	20
R762	RES	20
R763	RES	20
R764	RES	20
R765	RES	20
R766	RES	20
R767	RES	20

R768	RES	25
R769	RES	25
R770	RES	25
R771	RES	25
R772	RES	25
R773	RES	25
R774	RES	25
R777	RES	28
R779	RES	20
R786	RES	20
R787	RES	21
R788	RES	21
R789	RES	23
R790	RES	33
R791	RES	33
R792	RES	33
R794	RES	33
R795	RES	33
R796	RES	33
R797	RES	33
R798	RES	17
R806	RES	25
R807	RES	25
R808	RES	25
R817	RES	25
R818	RES	19
R819	RES	19
R823	RES	19
R824	RES	19
R825	RES	19
R826	RES	19
R827	RES	19
R828	RES	19
R829	RES	19
R830	RES	19
R832	RES	19
R833	RES	19
R835	RES	19
R836	RES	19
R837	RES	19
R838	RES	19
R839	RES	19
R840	RES	20
R841	RES	21
R842	RES	21
R843	RES	21
RP1	RPAK10P2C	18
RP2	RPAK4P	8
RP3	RPAK4P	8
RP4	RPAK4P	14
RP5	RPAK4P	14
RP6	RPAK4P	14
RP7	RPAK4P	14
RP8	RPAK4P	14
RP9	RPAK4P	9
RP10	RPAK4P	13
RP11	RPAK4P	14
RP12	RPAK4P	9
RP13	RPAK4P	14
RP14	RPAK4P	9
RP15	RPAK4P	14
RP16	RPAK4P	13
RP17	RPAK4P	9
RP18	RPAK4P	24
RP19	RPAK4P	24
RP20	RPAK4P	9
RP21	RPAK4P	24
RP22	RPAK4P	9
RP23	RPAK4P	24
RP24	RPAK4P	24
RP25	RPAK4P	24
RP26	RPAK4P	24
RP27	RPAK4P	24
RP28	RPAK4P	24
RP29	RPAK4P	9
RP30	RPAK4P	24
RP31	RPAK4P	9
RP32	RPAK4P	13
RP33	RPAK4P	12
RP34	RPAK4P	12
RP35	RPAK4P	13
RP36	RPAK4P	12
RP37	RPAK4P	27
RP38	RPAK4P	27
RP39	RPAK4P	29
RP40	RPAK10P2C	23
RP41	RPAK4P	29
RP42	RPAK10P2C	23
RP43	RPAK4P	17
RP44	RPAK4P	17
RP45	RPAK4P	17
RP46	RPAK10P2C	6
RP47	RPAK4P	14
RP49	RPAK4P	19
RP50	RPAK4P	19
RP51	RPAK4P	19
RP52	RPAK4P	19
RP53	RPAK2P	19
RP54	RPAK2P	19
RP55	RPAK2P	19
RP56	RPAK2P	19
RP57	RPAK2P	19
RP58	RPAK2P	19
RP59	RPAK2P	19
RP60	RPAK4P	19
SH1	SHLD_3P_EMI	4
U1	COMPARATOR_LMC7211	30
U2	NC7S32	22
U3	AMP_MAX4172	30
U4	PWR_CNTRL_TPS2211	18
U6	MAX1772	30
U7	MAX1717	33
U8	PCI5100GU	18
U9	SN74AUC1G08	6
U10	SN74AUC1G08	6
U11	FEPR_1MX8	9
U12	SN74AUC1G04	7
U13	LTC1625	31
U14	COMPARATOR_LMC7211	31
U15	P13B3257	33
U16	CBTV4020	10
U17	UPD720101_FBGA	17
U18	CBTV4020	10
U19	MAX1715	34
U20	NC7S32	29
U21	74LI25	23
U22	VREG_LP2951	31
U23	VREG_LP2951	31
U24	NC7S32	29
U25	NC7S32	29
U26	MAX6804	29
U27	CBTV4020	10
U28	CBTV4020	10
U29	M16C62	29
U30	CLK_GEN_CY25811	19
U31	CLK_GEN_CY28512	14
U32	LTC1778	20
U33	COMPARATOR_LMC7211	29
U34	VREG_MM1571J	21
U35	LTC3707	32
U36	TSB81BA3A	27
U37	VREG_LM2594	27
U38	VREG_LT1962	27
U39	74LG32	22
U40	74LG32	22
U42	COMPARATOR_LMC7211	22
U43	TRANSCEIVER_88E1111	26
U44	LTC1761	27
U45	LTC3405	26
U46	LTC3411	34
U47	RAGE_MBLTY_M10_CSP64_667	19 20 21
U48	TRA_SIE467BDQ	34
U49	VREG_LT1962	14
U50	TRA_SI3447DV	34
U51	INTREPID	8 9 12 13 14 15
U52	EEPROM_32KX8_M24256B	6
U53	ADT7460	25
U54	AT90S1200	6
U55	OPAMP_LMC7111	30
U56	APOLLO_MPC7445_360	5 6
U57	COMPARATOR_LMC7211	30
U58	SIL1162	19
U60	VREG_MM1571J	21
XW1	SHORT	30
XW2	SHORT	33
XW3	SHORT	31
XW4	SHORT	20
XW5	SHORT	20

XW6	SHORT	20
XW7	SHORT	21
XW8	SHORT	34
XW9	SHORT	20
XW10	SHORT	34
XW11	SHORT	20
XW12	SHORT	20
XW13	SHORT	32
XW14	SHORT	22
XW15	SHORT	22
XW17	SHORT	34
XW21	SHORT	34
XW23	SHORT	34
XW25	SHORT	34
XW27	SHORT	33
XW28	SHORT	33
XW29	SHORT	33
XW30	SHORT	25
XW31	SHORT	32
XW32	SHORT	32
XW34	SHORT	5
Y1	CRYSTAL	17
Y2	CRYSTAL	14
Y3	CRYSTAL_4PIN	29
Y4	CRYSTAL	29
Y5	CRYSTAL_4PIN	26
ZT1	HOLE_VIA	4
ZT2	HOLE_VIA	4
ZT3	HOLE_VIA	4
ZT4	HOLE_VIA	4
ZT5	HOLE_VIA	4
ZT6	HOLE_VIA	4
ZT7	HOLE_VIA	4
ZT8	HOLE_VIA	4
ZT9	HOLE_VIA	4
ZT10	HOLE_VIA	4
ZT11	HOLE_VIA	4
ZT12	HOLE_VIA	4
ZT13	HOLE_VIA	4
ZT14	HOLE_VIA	4
ZT15	HOLE_VIA	4
ZT16	HOLE_VIA	4
ZT17	HOLE_VIA	4
ZT18	HOLE_VIA	4
ZT19	HOLE_VIA	4
ZT20	HOLE_VIA	4
ZT21	HOLE_VIA	4
ZT22	HOLE_VIA	4
ZT23	HOLE_VIA	4
ZT24	HOLE_VIA	4
ZT25	HOLE_VIA	4
ZT26	HOLE_VIA	4
ZT27	HOLE_VIA	4
ZT28	HOLE_VIA	4
ZT29	HOLE_VIA	4
ZT30	HOLE_VIA	4
ZT31	HOLE_VIA	4
ZT32	HOLE_VIA	4
ZT33	HOLE_VIA	4
ZT34	HOLE_VIA	4
ZT35	HOLE_VIA	4
ZT36	HOLE_VIA	4
ZT37	HOLE_VIA	4
ZT38	HOLE_VIA	4
ZT39	HOLE_VIA	4
ZT40	HOLE_VIA	4
ZT41	HOLE_VIA	4
ZT42	HOLE_VIA	4
ZT43	HOLE_VIA	4
ZT44	HOLE_VIA	4
ZT45	HOLE_VIA	4
ZT46	HOLE_VIA	4
ZT47	HOLE_VIA	4
ZT48	HOLE_VIA	4
ZT49	HOLE_VIA	4
ZT50	HOLE_VIA	4
ZT51	HOLE_VIA	4
ZT52	HOLE_VIA	4
ZT53	HOLE_VIA	4
ZT54	HOLE_VIA	4
ZT55	HOLE_VIA	4
ZT56	HOLE_VIA	4
ZT57	HOLE_VIA	4
ZT58	HOLE_VIA	4
ZT59	HOLE_VIA	4
ZT60	HOLE_VIA	4
ZT61	HOLE_VIA	4
ZT62	HOLE_VIA	4
ZT63	HOLE_VIA	4
ZT64	HOLE_VIA	4
ZT65	HOLE_VIA	4
ZT66	HOLE_VIA	4
ZT67	HOLE_VIA	4
ZT68	HOLE_VIA	4
ZT69	HOLE_VIA	4
ZT70	HOLE_VIA	4
ZT71	HOLE_VIA	4
ZT72	HOLE_VIA	4
ZT73	HOLE_VIA	4
ZT74	HOLE_VIA	4
ZT75	HOLE_VIA	4
ZT76	HOLE_VIA	4
ZT77	HOLE_VIA	4
ZT78	HOLE_VIA	4
ZT79	HOLE_VIA	4
ZT80	HOLE_VIA	4
ZT81	HOLE_VIA	4
ZT82	HOLE_VIA	4
ZT83	HOLE_VIA	4
ZT84	HOLE_VIA	4
ZT85	HOLE_VIA	4
ZT86	HOLE_VIA	4